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ILI9326

a-Si TFT LCD Single Chip Driver
240RGBx432 Resolution and 262K color

Datasheet
Preliminary

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ILI TECHNOLOGY CORP.
8F, No.38, Taiyuan St., Jhubei City, Hsinchu County 302
Taiwan 300, R.O.C.
Tel.886-3-5600099; Fax.886-3-5600055
http://www.ilitek.com

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1. Introduction

ILI9326 is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 240RGBx432 dots, comprising 720-channel source driver, 432-channel gate driver, RAM for graphic display of 240RGBx432 dots, and power supply circuit.

ILI9326 has four kinds of system interfaces which are i80-system MPU interface (8-/9-/16-/18-bit bus width), VSYNC interface (system interface + VSYNC, internal clock, DB[17:0]), serial data transfer interface (SPI) and RGB 6-/16-/18-bit interface (DOTCLK, VSYNC, HSYNC, ENABLE, DB[17:0]).

In RGB interface and VSYNC interface mode, the combined use of high-speed RAM write function and widow address function enables to display a moving picture at a position specified by a user and still pictures in other areas on the screen simultaneously, which makes it possible to transfer display the refresh data only to minimize data transfers and power consumption.

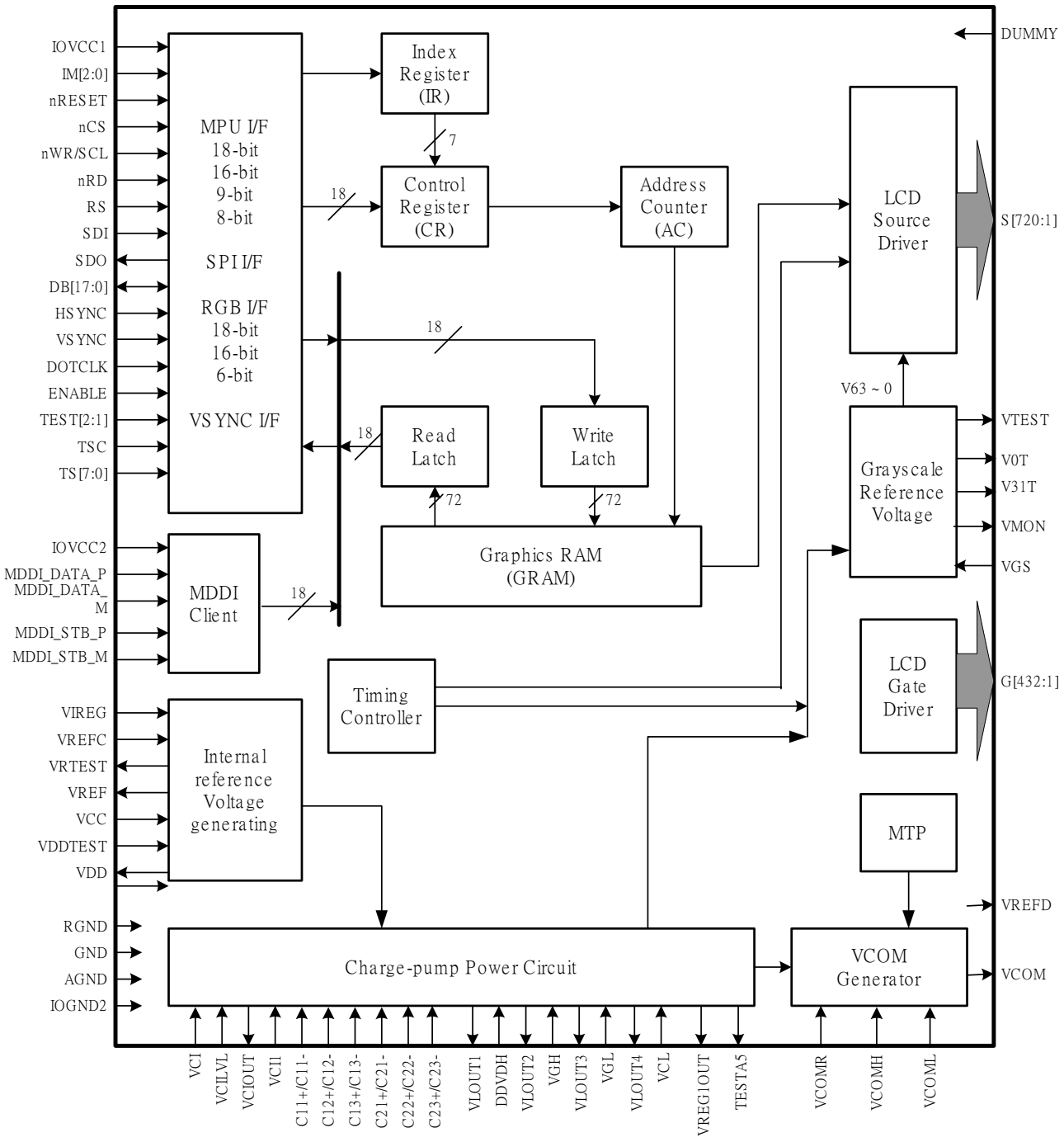
ILI9326 can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9326 also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9326 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, PDA and PMP where long battery life is a major concern.

2. Features

- Single chip solution for a liquid crystal WQVGA TFT LCD display
- 240RGBx432-dot resolution capable with real 262,144 display color
- Support MVA (Multi-domain Vertical Alignment) wide view display
- Incorporate 720-channel source driver and 432-channel gate driver
- Internal 233,280 bytes graphic RAM
- High-speed RAM burst write function
- System interfaces
  - i80 system interface with 8-/ 9-/16-/18-bit bus width
  - Serial Peripheral Interface (SPI)
  - RGB interface with 6-/16-/18-bit bus width (VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
  - VSYNC interface (System interface + VSYNC)
  - MDDI interface
- Internal oscillator and hardware reset
- Reversible source/gate driver shift direction
- Window address function to specify a rectangular area for internal GRAM access
- Abundant functions for color display control
  - γ-correction function enabling display in 262,144 colors
  - Line-unit vertical scrolling function

- Partial drive function, enabling partially driving an LCD panel at positions specified by user
- Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)
- Power saving functions
  - 8-color mode
  - standby mode
  - sleep mode
- Low -power consumption architecture
  - Low operating power supplies:
    - IOVCC1 = 1.65V ~ 3.3 V (interface I/O)
    - IOVCC2 = 2.5V ~ 3.3 V (MDDI interface)
    - Vcc = 2.4V ~ 3.3 V (internal logic)
    - Vci = 2.5V ~ 3.3 V (analog)
- LCD Voltage drive:
  - Source/VCOM power supply voltage
    - DVDH - GND = 4.5V ~ 6.0
    - VCL – GND = -2.0V ~ -3.0V
    - VCI – VCL $\leqq$ 6.0V
  - Gate driver output voltage
    - VGH - GND = 10V ~ 16V
    - VGL – GND = -5V ~ -15V
    - VGH – VGL $\leqq$ 32V
  - VCOM driver output voltage
    - VCOMH = 3.0V ~ (DDVDH-0.5)V
    - VCOML = (VCL+0.5)V ~ 0V
    - VCOMH-VCOML $\leqq$ 6.0V
- a-TFT LCD storage capacitor: Cst only

3. Block Diagram



4. Pin Descriptions

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><th colspan="4">Input Interface</th></tr>
<tr><td>IM2,
IM1,
IM0/ID</td><td>I</td><td>IOVCC1</td><td>Select the MPU system interface mode
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU-Interface Mode</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>i80-system 18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>i80-system 9-bit interface</td><td>DB[17:9]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>i80-system 16-bit interface</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>i80-system 8-bit interface</td><td>DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>ID</td><td>Serial Peripheral Interface (SPI)</td><td>SDI, SDO</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>MDDI interface</td><td></td></tr>
</table>
When the serial peripheral interface is selected, IM0 pin is used for the device code ID setting.</td></tr>
<tr><td>nCS</td><td>I</td><td>MPU
IOVCC1</td><td>A chip select signal.
Low: the ILI9326 is selected and accessible
High: the ILI9326 is not selected and not accessible
Fix to the IOVCC1 level when not in use.</td></tr>
<tr><td>RS</td><td>I</td><td>MPU
IOVCC1</td><td>A register select signal.
Low: select an index or status register
High: select a control register
Fix to GND level when not in use.</td></tr>
<tr><td>nWR/SCL</td><td>I</td><td>MPU
IOVCC1</td><td>A write strobe signal and enables an operation to write data when the signal is low.
Fix to either IOVCC1 level when not in use.

SPI Mode:
Synchronizing clock signal in SPI mode.</td></tr>
<tr><td>nRD</td><td>I</td><td>MPU
IOVCC1</td><td>A read strobe signal and enables an operation to read out data when the signal is low.
Fix to IOVCC1 level when not in use.</td></tr>
<tr><td>nRESET</td><td>I</td><td>MPU
IOVCC1</td><td>A reset pin.
Initializes the ILI9326 with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>SDI</td><td>I</td><td>MPU
IOVCC1</td><td>SPI interface input pin.
The data is latched on the rising edge of the SCL signal.
Fix to GND level when not in use.</td></tr>
<tr><td>SDO</td><td>O</td><td>MPU
IOVCC1</td><td>SPI interface output pin.
The data is outputted on the falling edge of the SCL signal.
Let SDO as floating when not used.</td></tr>
<tr><td>DB[17:0]</td><td>I/O</td><td>MPU
IOVCC1</td><td>18-bit parallel bi-directional data bus for MPU system interface mode
8-bit I/F: DB[17:10] is used.
9-bit I/F: DB[17:9] is used.
16-bit I/F: DB[17:10] and DB[8:1] is used.
18-bit I/F: DB[17:0] is used.

18-bit parallel bi-directional data bus for RGB interface operation
6-bit RGB I/F: DB[17:12] are used.
16-bit RGB I/F: DB[17:13] and DB[11:1] are used.
18-bit RGB I/F: DB[17:0] are used.

Unused pins must be fixed GND level.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>MPU
IOVCC1</td><td>Data ENEABLE signal for RGB interface operation.
Low: Select (access enabled)
High: Not select (access inhibited)
The EPL bit inverts the polarity of the ENABLE signal.</td></tr>
</table>

Pin Name	I/O	Type	Descriptions
			Fix to GND level when not in use.
DOTCLK	I	MPU IOVCC1	Dot clock signal for RGB interface operation. DPL = "0": Input data on the rising edge of DOTCLK DPL = "1": Input data on the falling edge of DOTCLK Fix to GND level when not in use.
VSYNC	I	MPU IOVCC1	Frame synchronizing signal for RGB interface operation. VSPL = "0": Active low. VSPL = "1": Active high. Fix to GND level when not in use.
HSYNC	I	MPU IOVCC1	Line synchronizing signal for RGB interface operation. HSPL = "0": Active low. HSPL = "1": Active high. Fix to GND level when not in use.
FMARK	O	MPU IOVCC1	Output a frame head pulse signal. The FMARK signal is used when writing RAM data in synchronization with frame. Leave the pin open when not in use.
TSC	I	IOVCC1	Sub display FLM signal, which is input from TSC when FMKM=1. Fix to GND level when not in use.
MDDI_DATA_P MDDI_DATA_M	I	MDDI IOVCC2	MDDI data signal lines. Data+ (MDDI_DATA_P) and data- (MDDI_DATA_M) are differential small swing signals. Make the wiring as short as possible so that the COG resistance becomes less 10 ohm. The specifications of interface must be compliant with the MDDI specification.
MDDI_STB_P MDDI_STB_M	I	MDDI IOVCC2	MDDI strobe signal lines. Stb+ (MDDI_STB_P) and Stb- (MDDI_STB_M) are differential small swing signals. Make the wiring as short as possible so that the COG resistance becomes less 10ohm. The specifications of interface must be compliant with the MDDI specification.
LCD Driving signals			
S720~S1	O	LCD	Source output voltage signals applied to liquid crystal. To change the shift direction of signal outputs, use the SS bit. SS = "0", the data in the RAM address "h00000" is output from S1. SS = "1", the data in the RAM address "h00000" is output from S720. S1, S4, S7, … display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).
G432~G1	O	LCD	Gate line output signals. VGH: the level selecting gate lines VGL: the level not selecting gate lines
VCOM	O	TFT common electrode	A supply voltage to the common electrode of TFT panel. VCOM is AC voltage alternating signal between the VCOMH and VCOML levels.
VCOMH	O	Stabilizing capacitor	The high level of VCOM AC voltage. Connect to a stabilizing capacitor.
VCOML	O	Stabilizing capacitor	The low level of VCOM AC voltage. Adjust the VCOML level with the VDV bits. Connect to a stabilizing capacitor.
VCOMR	-	-	Testing Pin. Please leave VCOMR as floating.
VGS	I	AGND or external resistor	Reference level for the grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor.
Charge-pump and Regulator Circuit			

Pin Name	I/O	Type	Descriptions
Vci	I	Power supply	A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.3V.
VciLVL	I	Power supply	VciLVL must be at the same voltage level as Vci. VciLVL=2.5V ~ 3.3V. Connect to the external power supply. In COG case, connect the VciLVL with Vci on the FPC to prevent noise.
VIREG	-	-	This pin is floating in ILI9326.
VPP1			MTP programming power When the MTP is programmed, provide VPP1=5Volt, and VPP3A=GND. If VPP1 is not used, let VPP1 as open.
VPP2			Test pins Leave these pins as open.
VPP3A			MTP programming ground. If VPP3A is not used, let VPP3A as open.
VPP3B			Test pins Leave these pins as open or connect VPP3B to GND.
VciOUT	O	Stabilizing capacitor Vci1	An internal reference voltage generated between Vci and AGND. The amplitude between Vci and GND is determined by the VC[2:0] bits.
Vci1	I	Stabilizing capacitor Vci1	An internal reference voltage for the step-up circuit1. The amplitude between Vci and GND is determined by the VC[2:0] bits. Make sure to set the Vci1 voltage so that the VLOUT1, VLOUT2, VLOUT3 and VLOUT4 voltages are set within the respective specification.
VLOUT1	O	Stabilizing capacitor, DDVDH	Output voltage from the step-up circuit 1, which is generated from Vci1. The step-up factor is set by “BT” bits. VLOUT1= 4.5 ~ 6.0V Place a stabilizing capacitor between AGND.
DDVDH	O	VLOUT1	Power supply for the source driver and Vcom drive. Connect to VLOUT1 and DDVDH = 4.5 ~ 6.0V
VLOUT2	O	Stabilizing capacitor, VGH	Output voltage from the step-up circuit 2, which is generated from Vci1 and DDVDH. The step-up factor is set by “BT” bits. VLOUT2= max.15V Place a stabilizing capacitor between AGND and a shottkey diode between Vci.
VGH	I	VLOUT2	Power supply for the gate driver, connect to VLOUT2.
VLOUT3	O	Stabilizing capacitor, VGL	Output voltage from the step-up circuit 2, which is generated from Vci1 and DDVDH. The step-up factor is set by “BT” bits. VLOUT3= max. -12.5V Place a stabilizing capacitor between AGND and a shottkey diode between Vci.
VGL	I	VLOUT3	Power supply for the gate driver, connect to VLOUT3.
VLOUT4	O	Stabilizing capacitor, VCL	Output voltage from the step-up circuit 2, which is generated from Vci1. VLOUT4 = -1.9V ~ -3.0V
VCL	I	Stabilizing capacitor, VCL	VcomL driver power supply. Connect to VLOUT4. VCL = 0 ~ –3.3V. Place a stabilizing capacitor between VCL and AGND
C11+, C11- C12+, C12-	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.
C13+, C13- C21+, C21- C22+, C22- C23+, C23-	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.
VREG1OUT	I/O	Stabilizing capacitor or power supply	Output voltage generated from the reference voltage. The voltage level is set with the VRH bits. VREG1OUT is (1) a source driver grayscale reference voltage, (2)

Pin Name	I/O	Type	Descriptions
			VcomH level reference voltage, and (3) Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 3.0 ~ (DDVDH – 0.5)V.
Vcc	I	Power supply	A supply voltage to the internal logic: Vcc = 2.4~3.3V Vcc ≧ IOVCC1, IOVCC2
GND	I	Power supply	GND for the logic side: GND = 0V.
RGND	I	Power supply	Internal RAM ground. RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.
VDD VDDOUT	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic circuit. Connect a stabilizing capacitor.
IOVCC1	I	Power supply	Power supply voltage to the interface pins: IM[2:0], nRESET, nCS, nWR, nRD, RS, DB[17:0], VSYNC, HSYNC, DOTCLK, ENABLE, SCL, SDI, SDO. IOVCC1 = 1.65 ~ 3.3V and Vcc ≧IOVCC1. In case of COG, connect to Vcc on the FPC if IOVCC1=Vcc, to prevent noise.
IOVCC2	I	Power supply	Power supply voltage to the MDDI pins: MDDI_DATA_P, MDDI_DATA_M, MDDI_STB_P and MDDI_STB_M. IOVCC2 = 2.5V ~ 3.3V and Vcc ≧IOVCC2. In case of COG, connect to Vcc on the FPC if IOVCC2=Vcc, to prevent noise.
IOGND2	I	Power supply	Power supply voltage to the MDDI pins: MDDI_DATA_P, MDDI_DATA_M, MDDI_STB_P and MDDI_STB_M. (IOGND2 = 0V) In case of COG, connect to GND on the FPC to prevent noise.
AGND	I	Power supply	AGND for the analog side: AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
Test Pads			
V0T, V31T	-	-	Test pins. Leave them open.
VTEST	-	-	Test pins. Leave them open.
VREFC	-	-	Test pins. Leave them open or connect VREFC to GND.
VREFD	-	-	Test pins. Leave them open or connect VREFD to GND.
VDDTEST	-	-	Test pins. Leave them open or connect VDDTEST to GND.
VMON	-	-	Test pins. Leave them open.
TESTA5	-	-	Test pins. Leave them open.
IOVCCDUM1~2	P	Power	Output the IOVCC1 voltage level. These pins are internally shorted to IOVCC1
VCCDUM1	-	-	Test pins. Leave them open.
IOGND2DUM1~8	P	Power	Output the GND voltage level. These pins are internally shorted to GND. When adjacent pins are needed to pull low, tie these pins to IOGND2DUM1~8.
GNDDUM1~19	P	Power	Output the GND voltage level. These pins are internally shorted to GND.
AGNDDUM1~5	O	Power	Output the GND voltage level. These pins are internally shorted to GND.
DUMMYR1~ 10	-	-	Dummy pads.
VGLDMY1~4	O	Open	Dummy pads. Leave these pins as open.
TESTO1~18	O	Open	Test pins. Leave them open.
TEST1~3	I	IOGND	Test pins (internal pull low). Connect to GND or leave these pins as open.

Liquid crystal power supply specifications Table 1

No.	Item		Description
1	TFT Source Driver		720 pins (240 x RGB)
2	TFT Gate Driver		432 pins
3	TFT Display's Capacitor Structure		Cst structure only (Common VCOM)
4	Liquid Crystal Drive Output	S1 ~ S720	V0 ~ V63 grayscales
		G1 ~ G432	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	IOVcc1	1.65 ~ 3.30V
		IOVcc2	2.50 ~ 3.30V
		Vcc	2.40 ~ 3.30V
		Vci	2.50 ~ 3.30V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6.0V
		VGH	10V ~ 20V
		VGL	-5V ~ -15V
		VCL	-1.9V ~ -3.0V
		VGH - VGL	Max. 32V
		Vci - VCL	Max. 6.0V
7	Internal Step-up Circuits	VLOUT1 (DDVDH)	Vci1 x2, x3
		VLOUT2 (VGH)	Vci1 x6, x7, x8
		VLOUT3 (VGL)	Vci1 x-3, x-4, x-5
		VCL	Vci1 x-1

5. Pad Arrangement and Coordination

Chip Size: 21550um x 906um

Chip thickness : 400 um or 280um(typ.)
Pad Location: Pad Center.

Coordinate Origin: Chip center

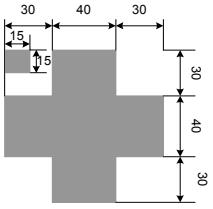
Au bump height: 15um (typ.)

Au Bump Size:

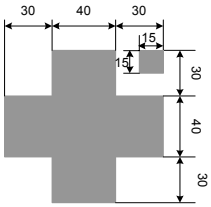
1. 18um x 110um (LCD Output Side: No. 300 ~ 1467)
   Gate: G1 ~ G320
   Source: S1 ~ S720

2. 50um x 80um (I/O Side: No. 1 ~ 299)
   Input Pads.

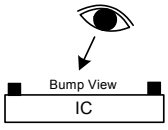
Alignment Mark: 1-a, 1-b.

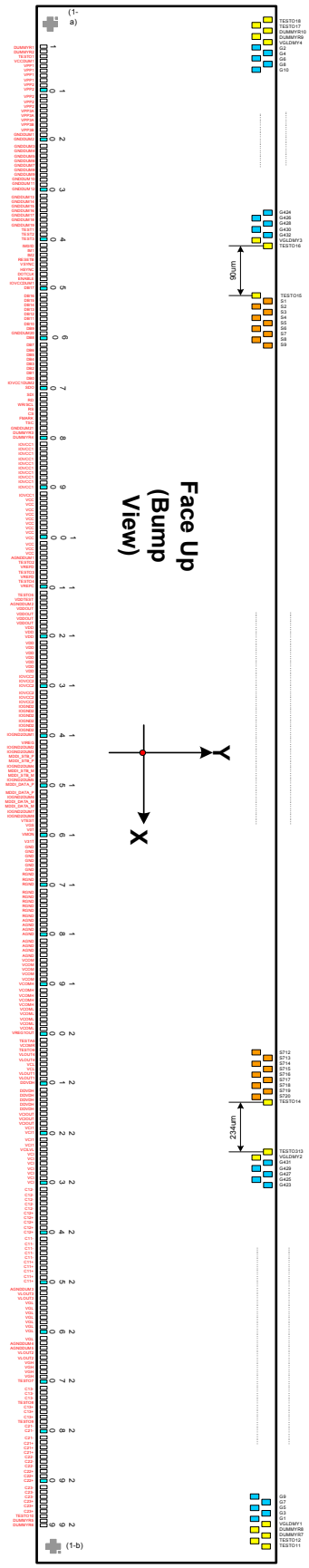


Alignment Mark: 1-a



Alignment Mark: 1-b





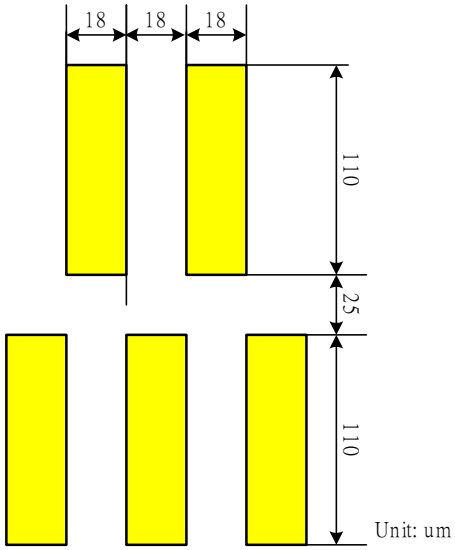
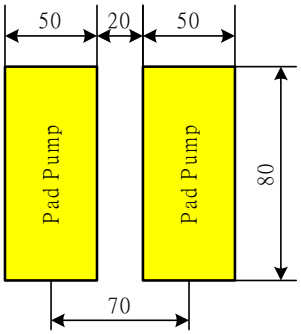
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	DUMMYR1	-10430.0	-359.0	61	DB7	-6230.0	-359.0	121	VDD	-2030.0	-359.0	181	AGND	2170.0	-359.0	241	C11-	6370.0	-359.0
2	DUMMYR2	-10360.0	-359.0	62	DB6	-6160.0	-359.0	122	VDD	-1960.0	-359.0	182	AGND	2240.0	-359.0	242	C11-	6440.0	-359.0
3	TESTO1	-10290.0	-359.0	63	DB5	-6090.0	-359.0	123	VDD	-1890.0	-359.0	183	AGND	2310.0	-359.0	243	C11-	6510.0	-359.0
4	VCCDUM1	-10220.0	-359.0	64	DB4	-6020.0	-359.0	124	VDD	-1820.0	-359.0	184	AGND	2380.0	-359.0	244	C11-	6580.0	-359.0
5	VPP1	-10150.0	-359.0	65	DB3	-5950.0	-359.0	125	VDD	-1750.0	-359.0	185	VCOM	2450.0	-359.0	245	C11-	6650.0	-359.0
6	VPP1	-10080.0	-359.0	66	DB2	-5880.0	-359.0	126	VDD	-1680.0	-359.0	186	VCOM	2520.0	-359.0	246	C11+	6720.0	-359.0
7	VPP1	-10010.0	-359.0	67	DB1	-5810.0	-359.0	127	VDD	-1610.0	-359.0	187	VCOM	2590.0	-359.0	247	C11+	6790.0	-359.0
8	VPP1	-9940.0	-359.0	68	DB0	-5740.0	-359.0	128	IOVCC2	-1540.0	-359.0	188	VCOM	2660.0	-359.0	248	C11+	6860.0	-359.0
9	VPP2	-9870.0	-359.0	69	IOVCC1DUM2	-5670.0	-359.0	129	IOVCC2	-1470.0	-359.0	189	VCOM	2730.0	-359.0	249	C11+	6930.0	-359.0
10	VPP2	-9800.0	-359.0	70	SDO	-5600.0	-359.0	130	IOVCC2	-1400.0	-359.0	190	VCOMH	2800.0	-359.0	250	C11+	7000.0	-359.0
11	VPP2	-9730.0	-359.0	71	SDI	-5530.0	-359.0	131	IOVCC2	-1330.0	-359.0	191	VCOMH	2870.0	-359.0	251	AGNDDUM3	7070.0	-359.0
12	VPP2	-9660.0	-359.0	72	RD	-5460.0	-359.0	132	IOVCC2	-1260.0	-359.0	192	VCOMH	2940.0	-359.0	252	VLOUT3	7140.0	-359.0
13	VPP2	-9590.0	-359.0	73	WR/SCL	-5390.0	-359.0	133	IOVCC2	-1190.0	-359.0	193	VCOMH	3010.0	-359.0	253	VLOUT3	7210.0	-359.0
14	VPP3A	-9520.0	-359.0	74	RS	-5320.0	-359.0	134	IOGND2	-1120.0	-359.0	194	VCOMH	3080.0	-359.0	254	VGL	7280.0	-359.0
15	VPP3A	-9450.0	-359.0	75	CS	-5250.0	-359.0	135	IOGND2	-1050.0	-359.0	195	VCOML	3150.0	-359.0	255	VGL	7350.0	-359.0
16	VPP3A	-9380.0	-359.0	76	FMARK	-5180.0	-359.0	136	IOGND2	-980.0	-359.0	196	VCOML	3220.0	-359.0	256	VGL	7420.0	-359.0
17	VPP3B	-9310.0	-359.0	77	TSC	-5110.0	-359.0	137	IOGND2	-910.0	-359.0	197	VCOML	3290.0	-359.0	257	VGL	7490.0	-359.0
18	VPP3B	-9240.0	-359.0	78	GNDDUM21	-5040.0	-359.0	138	IOGND2	-840.0	-359.0	198	VCOML	3360.0	-359.0	258	VGL	7560.0	-359.0
19	GNDDUM1	-9170.0	-359.0	79	DUMMYR3	-4970.0	-359.0	139	IOGND2	-770.0	-359.0	199	VCOML	3430.0	-359.0	259	VGL	7630.0	-359.0
20	GNDDUM2	-9100.0	-359.0	80	DUMMYR4	-4900.0	-359.0	140	IOGND2DUM1	-700.0	-359.0	200	VREG1OUT	3500.0	-359.0	260	VGL	7700.0	-359.0
21	GNDDUM3	-9030.0	-359.0	81	IOVCC1	-4830.0	-359.0	141	VIREG	-630.0	-359.0	201	TESTA5	3570.0	-359.0	261	VGL	7770.0	-359.0
22	GNDDUM4	-8960.0	-359.0	82	IOVCC1	-4760.0	-359.0	142	IOGND2DUM2	-560.0	-359.0	202	VCOMR	3640.0	-359.0	262	AGNDDUM4	7840.0	-359.0
23	GNDDUM5	-8890.0	-359.0	83	IOVCC1	-4690.0	-359.0	143	IOGND2DUM3	-490.0	-359.0	203	TESTO6	3710.0	-359.0	263	AGNDDUM5	7910.0	-359.0
24	GNDDUM6	-8820.0	-359.0	84	IOVCC1	-4620.0	-359.0	144	MDDI_STB_P	-420.0	-359.0	204	VLOUT4	3780.0	-359.0	264	VLOUT2	7980.0	-359.0
25	GNDDUM7	-8750.0	-359.0	85	IOVCC1	-4550.0	-359.0	145	MDDI_STB_P	-350.0	-359.0	205	VLOUT4	3850.0	-359.0	265	VLOUT2	8050.0	-359.0
26	GNDDUM8	-8680.0	-359.0	86	IOVCC1	-4480.0	-359.0	146	IOGND2DUM4	-280.0	-359.0	206	VCL	3920.0	-359.0	266	VGH	8120.0	-359.0
27	GNDDUM9	-8610.0	-359.0	87	IOVCC1	-4410.0	-359.0	147	MDDI_STB_M	-210.0	-359.0	207	VCL	3990.0	-359.0	267	VGH	8190.0	-359.0
28	GNDDUM10	-8540.0	-359.0	88	IOVCC1	-4340.0	-359.0	148	MDDI_STB_M	-140.0	-359.0	208	VLOUT1	4060.0	-359.0	268	VGH	8260.0	-359.0
29	GNDDUM11	-8470.0	-359.0	89	IOVCC1	-4270.0	-359.0	149	IOGND2DUM5	-70.0	-359.0	209	VLOUT1	4130.0	-359.0	269	VGH	8330.0	-359.0
30	GNDDUM12	-8400.0	-359.0	90	IOVCC1	-4200.0	-359.0	150	MDDI_DATA_P	0.0	-359.0	210	DDVDH	4200.0	-359.0	270	TESTO7	8400.0	-359.0
31	GNDDUM13	-8330.0	-359.0	91	IOVCC1	-4130.0	-359.0	151	MDDI_DATA_P	70.0	-359.0	211	DDVDH	4270.0	-359.0	271	C13-	8470.0	-359.0
32	GNDDUM14	-8260.0	-359.0	92	VCC	-4060.0	-359.0	152	IOGND2DUM6	140.0	-359.0	212	DDVDH	4340.0	-359.0	272	C13-	8540.0	-359.0
33	GNDDUM15	-8190.0	-359.0	93	VCC	-3990.0	-359.0	153	MDDI_DATA_M	210.0	-359.0	213	DDVDH	4410.0	-359.0	273	C13-	8610.0	-359.0
34	GNDDUM16	-8120.0	-359.0	94	VCC	-3920.0	-359.0	154	MDDI_DATA_M	280.0	-359.0	214	DDVDH	4480.0	-359.0	274	TESTO8	8680.0	-359.0
35	GNDDUM17	-8050.0	-359.0	95	VCC	-3850.0	-359.0	155	IOGND2DUM7	350.0	-359.0	215	DDVDH	4550.0	-359.0	275	C13+	8750.0	-359.0
36	GNDDUM18	-7980.0	-359.0	96	VCC	-3780.0	-359.0	156	IOGND2DUM8	420.0	-359.0	216	VCIOUT	4620.0	-359.0	276	C13+	8820.0	-359.0
37	GNDDUM19	-7910.0	-359.0	97	VCC	-3710.0	-359.0	157	VTEST	490.0	-359.0	217	VCIOUT	4690.0	-359.0	277	C13+	8890.0	-359.0
38	TEST1	-7840.0	-359.0	98	VCC	-3640.0	-359.0	158	VGS	560.0	-359.0	218	VCIOUT	4760.0	-359.0	278	TESTO9	8960.0	-359.0
39	TEST2	-7770.0	-359.0	99	VCC	-3570.0	-359.0	159	V0T	630.0	-359.0	219	VCI1	4830.0	-359.0	279	C21-	9030.0	-359.0
40	TEST3	-7700.0	-359.0	100	VCC	-3500.0	-359.0	160	VMON	700.0	-359.0	220	VCI1	4900.0	-359.0	280	C21-	9100.0	-359.0
41	IM0/ID	-7630.0	-359.0	101	VCC	-3430.0	-359.0	161	V31T	770.0	-359.0	221	VCI1	4970.0	-359.0	281	C21-	9170.0	-359.0
42	IM1	-7560.0	-359.0	102	VCC	-3360.0	-359.0	162	GND	840.0	-359.0	222	VCI1	5040.0	-359.0	282	C21+	9240.0	-359.0
43	IM2	-7490.0	-359.0	103	VCC	-3290.0	-359.0	163	GND	910.0	-359.0	223	VCILVL	5110.0	-359.0	283	C21+	9310.0	-359.0
44	RESETB	-7420.0	-359.0	104	AGNDDUM1	-3220.0	-359.0	164	GND	980.0	-359.0	224	VCI	5180.0	-359.0	284	C21+	9380.0	-359.0
45	VSYNC	-7350.0	-359.0	105	TESTO2	-3150.0	-359.0	165	GND	1050.0	-359.0	225	VCI	5250.0	-359.0	285	C22-	9450.0	-359.0
46	HSYNC	-7280.0	-359.0	106	VREFD	-3080.0	-359.0	166	GND	1120.0	-359.0	226	VCI	5320.0	-359.0	286	C22-	9520.0	-359.0
47	DOTCLK	-7210.0	-359.0	107	TESTO3	-3010.0	-359.0	167	GND	1190.0	-359.0	227	VCI	5390.0	-359.0	287	C22-	9590.0	-359.0
48	ENABLE	-7140.0	-359.0	108	VREFD	-2940.0	-359.0	168	RGND	1260.0	-359.0	228	VCI	5460.0	-359.0	288	C22+	9660.0	-359.0
49	IOVCCDUM1	-7070.0	-359.0	109	TESTO4	-2870.0	-359.0	169	RGND	1330.0	-359.0	229	VCI	5530.0	-359.0	289	C22+	9730.0	-359.0
50	DB17	-7000.0	-359.0	110	VREFC	-2800.0	-359.0	170	RGND	1400.0	-359.0	230	VCI	5600.0	-359.0	290	C22+	9800.0	-359.0
51	DB16	-6930.0	-359.0	111	TESTO5	-2730.0	-359.0	171	RGND	1470.0	-359.0	231	C12-	5670.0	-359.0	291	C23-	9870.0	-359.0
52	DB15	-6860.0	-359.0	112	VDDTEST	-2660.0	-359.0	172	RGND	1540.0	-359.0	232	C12-	5740.0	-359.0	292	C23-	9940.0	-359.0
53	DB14	-6790.0	-359.0	113	AGNDDUM2	-2590.0	-359.0	173	RGND	1610.0	-359.0	233	C12-	5810.0	-359.0	293	C23-	10010.0	-359.0
54	DB13	-6720.0	-359.0	114	VDDOUT	-2520.0	-359.0	174	RGND	1680.0	-359.0	234	C12-	5880.0	-359.0	294	C23+	10080.0	-359.0
55	DB12	-6650.0	-359.0	115	VDDOUT	-2450.0	-359.0	175	RGND	1750.0	-359.0	235	C12-	5950.0	-359.0	295	C23+	10150.0	-359.0
56	DB11	-6580.0	-359.0	116	VDDOUT	-2380.0	-359.0	176	RGND	1820.0	-359.0	236	C12+	6020.0	-359.0	296	C23+	10220.0	-359.0
57	DB10	-6510.0	-359.0	117	VDDOUT	-2310.0	-359.0	177	AGND	1890.0	-359.0	237	C12+	6090.0	-359.0	297	TESTO10	10290.0	-359.0
58	DB9	-6440.0	-359.0	118	VDD	-2240.0	-359.0	178	AGND	1960.0	-359.0	238	C12+	6160.0	-359.0	298	DUMMYR5	10360.0	-359.0
59	GNDDUM20	-6370.0	-359.0	119	VDD	-2170.0	-359.0	179	AGND	2030.0	-359.0	239	C12+	6230.0	-359.0	299	DUMMYR6	10430.0	-359.0
60	DB8	-6300.0	-359.0	120	VDD	-2100.0	-359.0	180	AGND	2100.0	-359.0	240	C12+	6300.0	-359.0	300	TESTO11	10647.0	340.0

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
301	TESTO12	10629.0	205.0	361	G113	9549.0	205.0	421	G233	8469.0	205.0	481	G353	7389.0	205.0	541	S703	6093.0	340.0
302	DUMMYR7	10611.0	340.0	362	G115	9531.0	340.0	422	G235	8451.0	340.0	482	G355	7371.0	340.0	542	S702	6075.0	205.0
303	DUMMYR8	10593.0	205.0	363	G117	9513.0	205.0	423	G237	8433.0	205.0	483	G357	7353.0	205.0	543	S701	6057.0	340.0
304	VGLDMY1	10575.0	340.0	364	G119	9495.0	340.0	424	G239	8415.0	340.0	484	G359	7335.0	340.0	544	S700	6039.0	205.0
305	G1	10557.0	205.0	365	G121	9477.0	205.0	425	G241	8397.0	205.0	485	G361	7317.0	205.0	545	S699	6021.0	340.0
306	G3	10539.0	340.0	366	G123	9459.0	340.0	426	G243	8379.0	340.0	486	G363	7299.0	340.0	546	S698	6003.0	205.0
307	G5	10521.0	205.0	367	G125	9441.0	205.0	427	G245	8361.0	205.0	487	G365	7281.0	205.0	547	S697	5985.0	340.0
308	G7	10503.0	340.0	368	G127	9423.0	340.0	428	G247	8343.0	340.0	488	G367	7263.0	340.0	548	S696	5967.0	205.0
309	G9	10485.0	205.0	369	G129	9405.0	205.0	429	G249	8325.0	205.0	489	G369	7245.0	205.0	549	S695	5949.0	340.0
310	G11	10467.0	340.0	370	G131	9387.0	340.0	430	G251	8307.0	340.0	490	G371	7227.0	340.0	550	S694	5931.0	205.0
311	G13	10449.0	205.0	371	G133	9369.0	205.0	431	G253	8289.0	205.0	491	G373	7209.0	205.0	551	S693	5913.0	340.0
312	G15	10431.0	340.0	372	G135	9351.0	340.0	432	G255	8271.0	340.0	492	G375	7191.0	340.0	552	S692	5895.0	205.0
313	G17	10413.0	205.0	373	G137	9333.0	205.0	433	G257	8253.0	205.0	493	G377	7173.0	205.0	553	S691	5877.0	340.0
314	G19	10395.0	340.0	374	G139	9315.0	340.0	434	G259	8235.0	340.0	494	G379	7155.0	340.0	554	S690	5859.0	205.0
315	G21	10377.0	205.0	375	G141	9297.0	205.0	435	G261	8217.0	205.0	495	G381	7137.0	205.0	555	S689	5841.0	340.0
316	G23	10359.0	340.0	376	G143	9279.0	340.0	436	G263	8199.0	340.0	496	G383	7119.0	340.0	556	S688	5823.0	205.0
317	G25	10341.0	205.0	377	G145	9261.0	205.0	437	G265	8181.0	205.0	497	G385	7101.0	205.0	557	S687	5805.0	340.0
318	G27	10323.0	340.0	378	G147	9243.0	340.0	438	G267	8163.0	340.0	498	G387	7083.0	340.0	558	S686	5787.0	205.0
319	G29	10305.0	205.0	379	G149	9225.0	205.0	439	G269	8145.0	205.0	499	G389	7065.0	205.0	559	S685	5769.0	340.0
320	G31	10287.0	340.0	380	G151	9207.0	340.0	440	G271	8127.0	340.0	500	G391	7047.0	340.0	560	S684	5751.0	205.0
321	G33	10269.0	205.0	381	G153	9189.0	205.0	441	G273	8109.0	205.0	501	G393	7029.0	205.0	561	S683	5733.0	340.0
322	G35	10251.0	340.0	382	G155	9171.0	340.0	442	G275	8091.0	340.0	502	G395	7011.0	340.0	562	S682	5715.0	205.0
323	G37	10233.0	205.0	383	G157	9153.0	205.0	443	G277	8073.0	205.0	503	G397	6993.0	205.0	563	S681	5697.0	340.0
324	G39	10215.0	340.0	384	G159	9135.0	340.0	444	G279	8055.0	340.0	504	G399	6975.0	340.0	564	S680	5679.0	205.0
325	G41	10197.0	205.0	385	G161	9117.0	205.0	445	G281	8037.0	205.0	505	G401	6957.0	205.0	565	S679	5661.0	340.0
326	G43	10179.0	340.0	386	G163	9099.0	340.0	446	G283	8019.0	340.0	506	G403	6939.0	340.0	566	S678	5643.0	205.0
327	G45	10161.0	205.0	387	G165	9081.0	205.0	447	G285	8001.0	205.0	507	G405	6921.0	205.0	567	S677	5625.0	340.0
328	G47	10143.0	340.0	388	G167	9063.0	340.0	448	G287	7983.0	340.0	508	G407	6903.0	340.0	568	S676	5607.0	205.0
329	G49	10125.0	205.0	389	G169	9045.0	205.0	449	G289	7965.0	205.0	509	G409	6885.0	205.0	569	S675	5589.0	340.0
330	G51	10107.0	340.0	390	G171	9027.0	340.0	450	G291	7947.0	340.0	510	G411	6867.0	340.0	570	S674	5571.0	205.0
331	G53	10089.0	205.0	391	G173	9009.0	205.0	451	G293	7929.0	205.0	511	G413	6849.0	205.0	571	S673	5553.0	340.0
332	G55	10071.0	340.0	392	G175	8991.0	340.0	452	G295	7911.0	340.0	512	G415	6831.0	340.0	572	S672	5535.0	205.0
333	G57	10053.0	205.0	393	G177	8973.0	205.0	453	G297	7893.0	205.0	513	G417	6813.0	205.0	573	S671	5517.0	340.0
334	G59	10035.0	340.0	394	G179	8955.0	340.0	454	G299	7875.0	340.0	514	G419	6795.0	340.0	574	S670	5499.0	205.0
335	G61	10017.0	205.0	395	G181	8937.0	205.0	455	G301	7857.0	205.0	515	G421	6777.0	205.0	575	S669	5481.0	340.0
336	G63	9999.0	340.0	396	G183	8919.0	340.0	456	G303	7839.0	340.0	516	G423	6759.0	340.0	576	S668	5463.0	205.0
337	G65	9981.0	205.0	397	G185	8901.0	205.0	457	G305	7821.0	205.0	517	G425	6741.0	205.0	577	S667	5445.0	340.0
338	G67	9963.0	340.0	398	G187	8883.0	340.0	458	G307	7803.0	340.0	518	G427	6723.0	340.0	578	S666	5427.0	205.0
339	G69	9945.0	205.0	399	G189	8865.0	205.0	459	G309	7785.0	205.0	519	G429	6705.0	205.0	579	S665	5409.0	340.0
340	G71	9927.0	340.0	400	G191	8847.0	340.0	460	G311	7767.0	340.0	520	G431	6687.0	340.0	580	S664	5391.0	205.0
341	G73	9909.0	205.0	401	G193	8829.0	205.0	461	G313	7749.0	205.0	521	VGLDMY2	6669.0	205.0	581	S663	5373.0	340.0
342	G75	9891.0	340.0	402	G195	8811.0	340.0	462	G315	7731.0	340.0	522	TESTO13	6651.0	340.0	582	S662	5355.0	205.0
343	G77	9873.0	205.0	403	G197	8793.0	205.0	463	G317	7713.0	205.0	523	TESTO14	6417.0	340.0	583	S661	5337.0	340.0
344	G79	9855.0	340.0	404	G199	8775.0	340.0	464	G319	7695.0	340.0	524	S720	6399.0	205.0	584	S660	5319.0	205.0
345	G81	9837.0	205.0	405	G201	8757.0	205.0	465	G321	7677.0	205.0	525	S719	6381.0	340.0	585	S659	5301.0	340.0
346	G83	9819.0	340.0	406	G203	8739.0	340.0	466	G323	7659.0	340.0	526	S718	6363.0	205.0	586	S658	5283.0	205.0
347	G85	9801.0	205.0	407	G205	8721.0	205.0	467	G325	7641.0	205.0	527	S717	6345.0	340.0	587	S657	5265.0	340.0
348	G87	9783.0	340.0	408	G207	8703.0	340.0	468	G327	7623.0	340.0	528	S716	6327.0	205.0	588	S656	5247.0	205.0
349	G89	9765.0	205.0	409	G209	8685.0	205.0	469	G329	7605.0	205.0	529	S715	6309.0	340.0	589	S655	5229.0	340.0
350	G91	9747.0	340.0	410	G211	8667.0	340.0	470	G331	7587.0	340.0	530	S714	6291.0	205.0	590	S654	5211.0	205.0
351	G93	9729.0	205.0	411	G213	8649.0	205.0	471	G333	7569.0	205.0	531	S713	6273.0	340.0	591	S653	5193.0	340.0
352	G95	9711.0	340.0	412	G215	8631.0	340.0	472	G335	7551.0	340.0	532	S712	6255.0	205.0	592	S652	5175.0	205.0
353	G97	9693.0	205.0	413	G217	8613.0	205.0	473	G337	7533.0	205.0	533	S711	6237.0	340.0	593	S651	5157.0	340.0
354	G99	9675.0	340.0	414	G219	8595.0	340.0	474	G339	7515.0	340.0	534	S710	6219.0	205.0	594	S650	5139.0	205.0
355	G101	9657.0	205.0	415	G221	8577.0	205.0	475	G341	7497.0	205.0	535	S709	6201.0	340.0	595	S649	5121.0	340.0
356	G103	9639.0	340.0	416	G223	8559.0	340.0	476	G343	7479.0	340.0	536	S708	6183.0	205.0	596	S648	5103.0	205.0
357	G105	9621.0	205.0	417	G225	8541.0	205.0	477	G345	7461.0	205.0	537	S707	6165.0	340.0	597	S647	5085.0	340.0
358	G107	9603.0	340.0	418	G227	8523.0	340.0	478	G347	7443.0	340.0	538	S706	6147.0	205.0	598	S646	5067.0	205.0
359	G109	9585.0	205.0	419	G229	8505.0	205.0	479	G349	7425.0	205.0	539	S705	6129.0	340.0	599	S645	5049.0	340.0
360	G111	9567.0	340.0	420	G231	8487.0	340.0	480	G351	7407.0	340.0	540	S704	6111.0	205.0	600	S644	5031.0	205.0

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
601	S643	5013.0	340.0	661	S583	3933.0	340.0	721	S523	2853.0	340.0	781	S463	1773.0	340.0	841	S403	693.0	340.0
602	S642	4995.0	205.0	662	S582	3915.0	205.0	722	S522	2835.0	205.0	782	S462	1755.0	205.0	842	S402	675.0	205.0
603	S641	4977.0	340.0	663	S581	3897.0	340.0	723	S521	2817.0	340.0	783	S461	1737.0	340.0	843	S401	657.0	340.0
604	S640	4959.0	205.0	664	S580	3879.0	205.0	724	S520	2799.0	205.0	784	S460	1719.0	205.0	844	S400	639.0	205.0
605	S639	4941.0	340.0	665	S579	3861.0	340.0	725	S519	2781.0	340.0	785	S459	1701.0	340.0	845	S399	621.0	340.0
606	S638	4923.0	205.0	666	S578	3843.0	205.0	726	S518	2763.0	205.0	786	S458	1683.0	205.0	846	S398	603.0	205.0
607	S637	4905.0	340.0	667	S577	3825.0	340.0	727	S517	2745.0	340.0	787	S457	1665.0	340.0	847	S397	585.0	340.0
608	S636	4887.0	205.0	668	S576	3807.0	205.0	728	S516	2727.0	205.0	788	S456	1647.0	205.0	848	S396	567.0	205.0
609	S635	4869.0	340.0	669	S575	3789.0	340.0	729	S515	2709.0	340.0	789	S455	1629.0	340.0	849	S395	549.0	340.0
610	S634	4851.0	205.0	670	S574	3771.0	205.0	730	S514	2691.0	205.0	790	S454	1611.0	205.0	850	S394	531.0	205.0
611	S633	4833.0	340.0	671	S573	3753.0	340.0	731	S513	2673.0	340.0	791	S453	1593.0	340.0	851	S393	513.0	340.0
612	S632	4815.0	205.0	672	S572	3735.0	205.0	732	S512	2655.0	205.0	792	S452	1575.0	205.0	852	S392	495.0	205.0
613	S631	4797.0	340.0	673	S571	3717.0	340.0	733	S511	2637.0	340.0	793	S451	1557.0	340.0	853	S391	477.0	340.0
614	S630	4779.0	205.0	674	S570	3699.0	205.0	734	S510	2619.0	205.0	794	S450	1539.0	205.0	854	S390	459.0	205.0
615	S629	4761.0	340.0	675	S569	3681.0	340.0	735	S509	2601.0	340.0	795	S449	1521.0	340.0	855	S389	441.0	340.0
616	S628	4743.0	205.0	676	S568	3663.0	205.0	736	S508	2583.0	205.0	796	S448	1503.0	205.0	856	S388	423.0	205.0
617	S627	4725.0	340.0	677	S567	3645.0	340.0	737	S507	2565.0	340.0	797	S447	1485.0	340.0	857	S387	405.0	340.0
618	S626	4707.0	205.0	678	S566	3627.0	205.0	738	S506	2547.0	205.0	798	S446	1467.0	205.0	858	S386	387.0	205.0
619	S625	4689.0	340.0	679	S565	3609.0	340.0	739	S505	2529.0	340.0	799	S445	1449.0	340.0	859	S385	369.0	340.0
620	S624	4671.0	205.0	680	S564	3591.0	205.0	740	S504	2511.0	205.0	800	S444	1431.0	205.0	860	S384	351.0	205.0
621	S623	4653.0	340.0	681	S563	3573.0	340.0	741	S503	2493.0	340.0	801	S443	1413.0	340.0	861	S383	333.0	340.0
622	S622	4635.0	205.0	682	S562	3555.0	205.0	742	S502	2475.0	205.0	802	S442	1395.0	205.0	862	S382	315.0	205.0
623	S621	4617.0	340.0	683	S561	3537.0	340.0	743	S501	2457.0	340.0	803	S441	1377.0	340.0	863	S381	297.0	340.0
624	S620	4599.0	205.0	684	S560	3519.0	205.0	744	S500	2439.0	205.0	804	S440	1359.0	205.0	864	S380	279.0	205.0
625	S619	4581.0	340.0	685	S559	3501.0	340.0	745	S499	2421.0	340.0	805	S439	1341.0	340.0	865	S379	261.0	340.0
626	S618	4563.0	205.0	686	S558	3483.0	205.0	746	S498	2403.0	205.0	806	S438	1323.0	205.0	866	S378	243.0	205.0
627	S617	4545.0	340.0	687	S557	3465.0	340.0	747	S497	2385.0	340.0	807	S437	1305.0	340.0	867	S377	225.0	340.0
628	S616	4527.0	205.0	688	S556	3447.0	205.0	748	S496	2367.0	205.0	808	S436	1287.0	205.0	868	S376	207.0	205.0
629	S615	4509.0	340.0	689	S555	3429.0	340.0	749	S495	2349.0	340.0	809	S435	1269.0	340.0	869	S375	189.0	340.0
630	S614	4491.0	205.0	690	S554	3411.0	205.0	750	S494	2331.0	205.0	810	S434	1251.0	205.0	870	S374	171.0	205.0
631	S613	4473.0	340.0	691	S553	3393.0	340.0	751	S493	2313.0	340.0	811	S433	1233.0	340.0	871	S373	153.0	340.0
632	S612	4455.0	205.0	692	S552	3375.0	205.0	752	S492	2295.0	205.0	812	S432	1215.0	205.0	872	S372	135.0	205.0
633	S611	4437.0	340.0	693	S551	3357.0	340.0	753	S491	2277.0	340.0	813	S431	1197.0	340.0	873	S371	117.0	340.0
634	S610	4419.0	205.0	694	S550	3339.0	205.0	754	S490	2259.0	205.0	814	S430	1179.0	205.0	874	S370	99.0	205.0
635	S609	4401.0	340.0	695	S549	3321.0	340.0	755	S489	2241.0	340.0	815	S429	1161.0	340.0	875	S369	81.0	340.0
636	S608	4383.0	205.0	696	S548	3303.0	205.0	756	S488	2223.0	205.0	816	S428	1143.0	205.0	876	S368	63.0	205.0
637	S607	4365.0	340.0	697	S547	3285.0	340.0	757	S487	2205.0	340.0	817	S427	1125.0	340.0	877	S367	45.0	340.0
638	S606	4347.0	205.0	698	S546	3267.0	205.0	758	S486	2187.0	205.0	818	S426	1107.0	205.0	878	S366	27.0	205.0
639	S605	4329.0	340.0	699	S545	3249.0	340.0	759	S485	2169.0	340.0	819	S425	1089.0	340.0	879	S365	9.0	340.0
640	S604	4311.0	205.0	700	S544	3231.0	205.0	760	S484	2151.0	205.0	820	S424	1071.0	205.0	880	S364	-9.0	205.0
641	S603	4293.0	340.0	701	S543	3213.0	340.0	761	S483	2133.0	340.0	821	S423	1053.0	340.0	881	S363	-27.0	340.0
642	S602	4275.0	205.0	702	S542	3195.0	205.0	762	S482	2115.0	205.0	822	S422	1035.0	205.0	882	S362	-45.0	205.0
643	S601	4257.0	340.0	703	S541	3177.0	340.0	763	S481	2097.0	340.0	823	S421	1017.0	340.0	883	S361	-63.0	340.0
644	S600	4239.0	205.0	704	S540	3159.0	205.0	764	S480	2079.0	205.0	824	S420	999.0	205.0	884	S360	-81.0	205.0
645	S599	4221.0	340.0	705	S539	3141.0	340.0	765	S479	2061.0	340.0	825	S419	981.0	340.0	885	S359	-99.0	340.0
646	S598	4203.0	205.0	706	S538	3123.0	205.0	766	S478	2043.0	205.0	826	S418	963.0	205.0	886	S358	-117.0	205.0
647	S597	4185.0	340.0	707	S537	3105.0	340.0	767	S477	2025.0	340.0	827	S417	945.0	340.0	887	S357	-135.0	340.0
648	S596	4167.0	205.0	708	S536	3087.0	205.0	768	S476	2007.0	205.0	828	S416	927.0	205.0	888	S356	-153.0	205.0
649	S595	4149.0	340.0	709	S535	3069.0	340.0	769	S475	1989.0	340.0	829	S415	909.0	340.0	889	S355	-171.0	340.0
650	S594	4131.0	205.0	710	S534	3051.0	205.0	770	S474	1971.0	205.0	830	S414	891.0	205.0	890	S354	-189.0	205.0
651	S593	4113.0	340.0	711	S533	3033.0	340.0	771	S473	1953.0	340.0	831	S413	873.0	340.0	891	S353	-207.0	340.0
652	S592	4095.0	205.0	712	S532	3015.0	205.0	772	S472	1935.0	205.0	832	S412	855.0	205.0	892	S352	-225.0	205.0
653	S591	4077.0	340.0	713	S531	2997.0	340.0	773	S471	1917.0	340.0	833	S411	837.0	340.0	893	S351	-243.0	340.0
654	S590	4059.0	205.0	714	S530	2979.0	205.0	774	S470	1899.0	205.0	834	S410	819.0	205.0	894	S350	-261.0	205.0
655	S589	4041.0	340.0	715	S529	2961.0	340.0	775	S469	1881.0	340.0	835	S409	801.0	340.0	895	S349	-279.0	340.0
656	S588	4023.0	205.0	716	S528	2943.0	205.0	776	S468	1863.0	205.0	836	S408	783.0	205.0	896	S348	-297.0	205.0
657	S587	4005.0	340.0	717	S527	2925.0	340.0	777	S467	1845.0	340.0	837	S407	765.0	340.0	897	S347	-315.0	340.0
658	S586	3987.0	205.0	718	S526	2907.0	205.0	778	S466	1827.0	205.0	838	S406	747.0	205.0	898	S346	-333.0	205.0
659	S585	3969.0	340.0	719	S525	2889.0	340.0	779	S465	1809.0	340.0	839	S405	729.0	340.0	899	S345	-351.0	340.0
660	S584	3951.0	205.0	720	S524	2871.0	205.0	780	S464	1791.0	205.0	840	S404	711.0	205.0	900	S344	-369.0	205.0

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
901	S343	-387.0	340.0	961	S283	-1467.0	340.0	1021	S223	-2547.0	340.0	1081	S163	-3627.0	340.0	1141	S103	-4707.0	340.0
902	S342	-405.0	205.0	962	S282	-1485.0	205.0	1022	S222	-2565.0	205.0	1082	S162	-3645.0	205.0	1142	S102	-4725.0	205.0
903	S341	-423.0	340.0	963	S281	-1503.0	340.0	1023	S221	-2583.0	340.0	1083	S161	-3663.0	340.0	1143	S101	-4743.0	340.0
904	S340	-441.0	205.0	964	S280	-1521.0	205.0	1024	S220	-2601.0	205.0	1084	S160	-3681.0	205.0	1144	S100	-4761.0	205.0
905	S339	-459.0	340.0	965	S279	-1539.0	340.0	1025	S219	-2619.0	340.0	1085	S159	-3699.0	340.0	1145	S99	-4779.0	340.0
906	S338	-477.0	205.0	966	S278	-1557.0	205.0	1026	S218	-2637.0	205.0	1086	S158	-3717.0	205.0	1146	S98	-4797.0	205.0
907	S337	-495.0	340.0	967	S277	-1575.0	340.0	1027	S217	-2655.0	340.0	1087	S157	-3735.0	340.0	1147	S97	-4815.0	340.0
908	S336	-513.0	205.0	968	S276	-1593.0	205.0	1028	S216	-2673.0	205.0	1088	S156	-3753.0	205.0	1148	S96	-4833.0	205.0
909	S335	-531.0	340.0	969	S275	-1611.0	340.0	1029	S215	-2691.0	340.0	1089	S155	-3771.0	340.0	1149	S95	-4851.0	340.0
910	S334	-549.0	205.0	970	S274	-1629.0	205.0	1030	S214	-2709.0	205.0	1090	S154	-3789.0	205.0	1150	S94	-4869.0	205.0
911	S333	-567.0	340.0	971	S273	-1647.0	340.0	1031	S213	-2727.0	340.0	1091	S153	-3807.0	340.0	1151	S93	-4887.0	340.0
912	S332	-585.0	205.0	972	S272	-1665.0	205.0	1032	S212	-2745.0	205.0	1092	S152	-3825.0	205.0	1152	S92	-4905.0	205.0
913	S331	-603.0	340.0	973	S271	-1683.0	340.0	1033	S211	-2763.0	340.0	1093	S151	-3843.0	340.0	1153	S91	-4923.0	340.0
914	S330	-621.0	205.0	974	S270	-1701.0	205.0	1034	S210	-2781.0	205.0	1094	S150	-3861.0	205.0	1154	S90	-4941.0	205.0
915	S329	-639.0	340.0	975	S269	-1719.0	340.0	1035	S209	-2799.0	340.0	1095	S149	-3879.0	340.0	1155	S89	-4959.0	340.0
916	S328	-657.0	205.0	976	S268	-1737.0	205.0	1036	S208	-2817.0	205.0	1096	S148	-3897.0	205.0	1156	S88	-4977.0	205.0
917	S327	-675.0	340.0	977	S267	-1755.0	340.0	1037	S207	-2835.0	340.0	1097	S147	-3915.0	340.0	1157	S87	-4995.0	340.0
918	S326	-693.0	205.0	978	S266	-1773.0	205.0	1038	S206	-2853.0	205.0	1098	S146	-3933.0	205.0	1158	S86	-5013.0	205.0
919	S325	-711.0	340.0	979	S265	-1791.0	340.0	1039	S205	-2871.0	340.0	1099	S145	-3951.0	340.0	1159	S85	-5031.0	340.0
920	S324	-729.0	205.0	980	S264	-1809.0	205.0	1040	S204	-2889.0	205.0	1100	S144	-3969.0	205.0	1160	S84	-5049.0	205.0
921	S323	-747.0	340.0	981	S263	-1827.0	340.0	1041	S203	-2907.0	340.0	1101	S143	-3987.0	340.0	1161	S83	-5067.0	340.0
922	S322	-765.0	205.0	982	S262	-1845.0	205.0	1042	S202	-2925.0	205.0	1102	S142	-4005.0	205.0	1162	S82	-5085.0	205.0
923	S321	-783.0	340.0	983	S261	-1863.0	340.0	1043	S201	-2943.0	340.0	1103	S141	-4023.0	340.0	1163	S81	-5103.0	340.0
924	S320	-801.0	205.0	984	S260	-1881.0	205.0	1044	S200	-2961.0	205.0	1104	S140	-4041.0	205.0	1164	S80	-5121.0	205.0
925	S319	-819.0	340.0	985	S259	-1899.0	340.0	1045	S199	-2979.0	340.0	1105	S139	-4059.0	340.0	1165	S79	-5139.0	340.0
926	S318	-837.0	205.0	986	S258	-1917.0	205.0	1046	S198	-2997.0	205.0	1106	S138	-4077.0	205.0	1166	S78	-5157.0	205.0
927	S317	-855.0	340.0	987	S257	-1935.0	340.0	1047	S197	-3015.0	340.0	1107	S137	-4095.0	340.0	1167	S77	-5175.0	340.0
928	S316	-873.0	205.0	988	S256	-1953.0	205.0	1048	S196	-3033.0	205.0	1108	S136	-4113.0	205.0	1168	S76	-5193.0	205.0
929	S315	-891.0	340.0	989	S255	-1971.0	340.0	1049	S195	-3051.0	340.0	1109	S135	-4131.0	340.0	1169	S75	-5211.0	340.0
930	S314	-909.0	205.0	990	S254	-1989.0	205.0	1050	S194	-3069.0	205.0	1110	S134	-4149.0	205.0	1170	S74	-5229.0	205.0
931	S313	-927.0	340.0	991	S253	-2007.0	340.0	1051	S193	-3087.0	340.0	1111	S133	-4167.0	340.0	1171	S73	-5247.0	340.0
932	S312	-945.0	205.0	992	S252	-2025.0	205.0	1052	S192	-3105.0	205.0	1112	S132	-4185.0	205.0	1172	S72	-5265.0	205.0
933	S311	-963.0	340.0	993	S251	-2043.0	340.0	1053	S191	-3123.0	340.0	1113	S131	-4203.0	340.0	1173	S71	-5283.0	340.0
934	S310	-981.0	205.0	994	S250	-2061.0	205.0	1054	S190	-3141.0	205.0	1114	S130	-4221.0	205.0	1174	S70	-5301.0	205.0
935	S309	-999.0	340.0	995	S249	-2079.0	340.0	1055	S189	-3159.0	340.0	1115	S129	-4239.0	340.0	1175	S69	-5319.0	340.0
936	S308	-1017.0	205.0	996	S248	-2097.0	205.0	1056	S188	-3177.0	205.0	1116	S128	-4257.0	205.0	1176	S68	-5337.0	205.0
937	S307	-1035.0	340.0	997	S247	-2115.0	340.0	1057	S187	-3195.0	340.0	1117	S127	-4275.0	340.0	1177	S67	-5355.0	340.0
938	S306	-1053.0	205.0	998	S246	-2133.0	205.0	1058	S186	-3213.0	205.0	1118	S126	-4293.0	205.0	1178	S66	-5373.0	205.0
939	S305	-1071.0	340.0	999	S245	-2151.0	340.0	1059	S185	-3231.0	340.0	1119	S125	-4311.0	340.0	1179	S65	-5391.0	340.0
940	S304	-1089.0	205.0	1000	S244	-2169.0	205.0	1060	S184	-3249.0	205.0	1120	S124	-4329.0	205.0	1180	S64	-5409.0	205.0
941	S303	-1107.0	340.0	1001	S243	-2187.0	340.0	1061	S183	-3267.0	340.0	1121	S123	-4347.0	340.0	1181	S63	-5427.0	340.0
942	S302	-1125.0	205.0	1002	S242	-2205.0	205.0	1062	S182	-3285.0	205.0	1122	S122	-4365.0	205.0	1182	S62	-5445.0	205.0
943	S301	-1143.0	340.0	1003	S241	-2223.0	340.0	1063	S181	-3303.0	340.0	1123	S121	-4383.0	340.0	1183	S61	-5463.0	340.0
944	S300	-1161.0	205.0	1004	S240	-2241.0	205.0	1064	S180	-3321.0	205.0	1124	S120	-4401.0	205.0	1184	S60	-5481.0	205.0
945	S299	-1179.0	340.0	1005	S239	-2259.0	340.0	1065	S179	-3339.0	340.0	1125	S119	-4419.0	340.0	1185	S59	-5499.0	340.0
946	S298	-1197.0	205.0	1006	S238	-2277.0	205.0	1066	S178	-3357.0	205.0	1126	S118	-4437.0	205.0	1186	S58	-5517.0	205.0
947	S297	-1215.0	340.0	1007	S237	-2295.0	340.0	1067	S177	-3375.0	340.0	1127	S117	-4455.0	340.0	1187	S57	-5535.0	340.0
948	S296	-1233.0	205.0	1008	S236	-2313.0	205.0	1068	S176	-3393.0	205.0	1128	S116	-4473.0	205.0	1188	S56	-5553.0	205.0
949	S295	-1251.0	340.0	1009	S235	-2331.0	340.0	1069	S175	-3411.0	340.0	1129	S115	-4491.0	340.0	1189	S55	-5571.0	340.0
950	S294	-1269.0	205.0	1010	S234	-2349.0	205.0	1070	S174	-3429.0	205.0	1130	S114	-4509.0	205.0	1190	S54	-5589.0	205.0
951	S293	-1287.0	340.0	1011	S233	-2367.0	340.0	1071	S173	-3447.0	340.0	1131	S113	-4527.0	340.0	1191	S53	-5607.0	340.0
952	S292	-1305.0	205.0	1012	S232	-2385.0	205.0	1072	S172	-3465.0	205.0	1132	S112	-4545.0	205.0	1192	S52	-5625.0	205.0
953	S291	-1323.0	340.0	1013	S231	-2403.0	340.0	1073	S171	-3483.0	340.0	1133	S111	-4563.0	340.0	1193	S51	-5643.0	340.0
954	S290	-1341.0	205.0	1014	S230	-2421.0	205.0	1074	S170	-3501.0	205.0	1134	S110	-4581.0	205.0	1194	S50	-5661.0	205.0
955	S289	-1359.0	340.0	1015	S229	-2439.0	340.0	1075	S169	-3519.0	340.0	1135	S109	-4599.0	340.0	1195	S49	-5679.0	340.0
956	S288	-1377.0	205.0	1016	S228	-2457.0	205.0	1076	S168	-3537.0	205.0	1136	S108	-4617.0	205.0	1196	S48	-5697.0	205.0
957	S287	-1395.0	340.0	1017	S227	-2475.0	340.0	1077	S167	-3555.0	340.0	1137	S107	-4635.0	340.0	1197	S47	-5715.0	340.0
958	S286	-1413.0	205.0	1018	S226	-2493.0	205.0	1078	S166	-3573.0	205.0	1138	S106	-4653.0	205.0	1198	S46	-5733.0	205.0
959	S285	-1431.0	340.0	1019	S225	-2511.0	340.0	1079	S165	-3591.0	340.0	1139	S105	-4671.0	340.0	1199	S45	-5751.0	340.0
960	S284	-1449.0	205.0	1020	S224	-2529.0	205.0	1080	S164	-3609.0	205.0	1140	S104	-4689.0	205.0	1200	S44	-5769.0	205.0

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1201	S43	-5787.0	340.0	1261	G404	-6939.0	340.0	1321	G284	-8019.0	340.0	1381	G164	-9099.0	340.0	1441	G44	-10179.0	340.0
1202	S42	-5805.0	205.0	1262	G402	-6957.0	205.0	1322	G282	-8037.0	205.0	1382	G162	-9117.0	205.0	1442	G42	-10197.0	205.0
1203	S41	-5823.0	340.0	1263	G400	-6975.0	340.0	1323	G280	-8055.0	340.0	1383	G160	-9135.0	340.0	1443	G40	-10215.0	340.0
1204	S40	-5841.0	205.0	1264	G398	-6993.0	205.0	1324	G278	-8073.0	205.0	1384	G158	-9153.0	205.0	1444	G38	-10233.0	205.0
1205	S39	-5859.0	340.0	1265	G396	-7011.0	340.0	1325	G276	-8091.0	340.0	1385	G156	-9171.0	340.0	1445	G36	-10251.0	340.0
1206	S38	-5877.0	205.0	1266	G394	-7029.0	205.0	1326	G274	-8109.0	205.0	1386	G154	-9189.0	205.0	1446	G34	-10269.0	205.0
1207	S37	-5895.0	340.0	1267	G392	-7047.0	340.0	1327	G272	-8127.0	340.0	1387	G152	-9207.0	340.0	1447	G32	-10287.0	340.0
1208	S36	-5913.0	205.0	1268	G390	-7065.0	205.0	1328	G270	-8145.0	205.0	1388	G150	-9225.0	205.0	1448	G30	-10305.0	205.0
1209	S35	-5931.0	340.0	1269	G388	-7083.0	340.0	1329	G268	-8163.0	340.0	1389	G148	-9243.0	340.0	1449	G28	-10323.0	340.0
1210	S34	-5949.0	205.0	1270	G386	-7101.0	205.0	1330	G266	-8181.0	205.0	1390	G146	-9261.0	205.0	1450	G26	-10341.0	205.0
1211	S33	-5967.0	340.0	1271	G384	-7119.0	340.0	1331	G264	-8199.0	340.0	1391	G144	-9279.0	340.0	1451	G24	-10359.0	340.0
1212	S32	-5985.0	205.0	1272	G382	-7137.0	205.0	1332	G262	-8217.0	205.0	1392	G142	-9297.0	205.0	1452	G22	-10377.0	205.0
1213	S31	-6003.0	340.0	1273	G380	-7155.0	340.0	1333	G260	-8235.0	340.0	1393	G140	-9315.0	340.0	1453	G20	-10395.0	340.0
1214	S30	-6021.0	205.0	1274	G378	-7173.0	205.0	1334	G258	-8253.0	205.0	1394	G138	-9333.0	205.0	1454	G18	-10413.0	205.0
1215	S29	-6039.0	340.0	1275	G376	-7191.0	340.0	1335	G256	-8271.0	340.0	1395	G136	-9351.0	340.0	1455	G16	-10431.0	340.0
1216	S28	-6057.0	205.0	1276	G374	-7209.0	205.0	1336	G254	-8289.0	205.0	1396	G134	-9369.0	205.0	1456	G14	-10449.0	205.0
1217	S27	-6075.0	340.0	1277	G372	-7227.0	340.0	1337	G252	-8307.0	340.0	1397	G132	-9387.0	340.0	1457	G12	-10467.0	340.0
1218	S26	-6093.0	205.0	1278	G370	-7245.0	205.0	1338	G250	-8325.0	205.0	1398	G130	-9405.0	205.0	1458	G10	-10485.0	205.0
1219	S25	-6111.0	340.0	1279	G368	-7263.0	340.0	1339	G248	-8343.0	340.0	1399	G128	-9423.0	340.0	1459	G8	-10503.0	340.0
1220	S24	-6129.0	205.0	1280	G366	-7281.0	205.0	1340	G246	-8361.0	205.0	1400	G126	-9441.0	205.0	1460	G6	-10521.0	205.0
1221	S23	-6147.0	340.0	1281	G364	-7299.0	340.0	1341	G244	-8379.0	340.0	1401	G124	-9459.0	340.0	1461	G4	-10539.0	340.0
1222	S22	-6165.0	205.0	1282	G362	-7317.0	205.0	1342	G242	-8397.0	205.0	1402	G122	-9477.0	205.0	1462	G2	-10557.0	205.0
1223	S21	-6183.0	340.0	1283	G360	-7335.0	340.0	1343	G240	-8415.0	340.0	1403	G120	-9495.0	340.0	1463	VGLDMY4	-10575.0	340.0
1224	S20	-6201.0	205.0	1284	G358	-7353.0	205.0	1344	G238	-8433.0	205.0	1404	G118	-9513.0	205.0	1464	DUMMYR9	-10593.0	205.0
1225	S19	-6219.0	340.0	1285	G356	-7371.0	340.0	1345	G236	-8451.0	340.0	1405	G116	-9531.0	340.0	1465	DUMMY10	-10611.0	340.0
1226	S18	-6237.0	205.0	1286	G354	-7389.0	205.0	1346	G234	-8469.0	205.0	1406	G114	-9549.0	205.0	1466	TESTO17	-10629.0	205.0
1227	S17	-6255.0	340.0	1287	G352	-7407.0	340.0	1347	G232	-8487.0	340.0	1407	G112	-9567.0	340.0	1467	TESTO18	-10647.0	340.0
1228	S16	-6273.0	205.0	1288	G350	-7425.0	205.0	1348	G230	-8505.0	205.0	1408	G110	-9585.0	205.0				
1229	S15	-6291.0	340.0	1289	G348	-7443.0	340.0	1349	G228	-8523.0	340.0	1409	G108	-9603.0	340.0				
1230	S14	-6309.0	205.0	1290	G346	-7461.0	205.0	1350	G226	-8541.0	205.0	1410	G106	-9621.0	205.0				
1231	S13	-6327.0	340.0	1291	G344	-7479.0	340.0	1351	G224	-8559.0	340.0	1411	G104	-9639.0	340.0				
1232	S12	-6345.0	205.0	1292	G342	-7497.0	205.0	1352	G222	-8577.0	205.0	1412	G102	-9657.0	205.0				
1233	S11	-6363.0	340.0	1293	G340	-7515.0	340.0	1353	G220	-8595.0	340.0	1413	G100	-9675.0	340.0				
1234	S10	-6381.0	205.0	1294	G338	-7533.0	205.0	1354	G218	-8613.0	205.0	1414	G98	-9693.0	205.0				
1235	S9	-6399.0	340.0	1295	G336	-7551.0	340.0	1355	G216	-8631.0	340.0	1415	G96	-9711.0	340.0				
1236	S8	-6417.0	205.0	1296	G334	-7569.0	205.0	1356	G214	-8649.0	205.0	1416	G94	-9729.0	205.0				
1237	S7	-6435.0	340.0	1297	G332	-7587.0	340.0	1357	G212	-8667.0	340.0	1417	G92	-9747.0	340.0				
1238	S6	-6453.0	205.0	1298	G330	-7605.0	205.0	1358	G210	-8685.0	205.0	1418	G90	-9765.0	205.0				
1239	S5	-6471.0	340.0	1299	G328	-7623.0	340.0	1359	G208	-8703.0	340.0	1419	G88	-9783.0	340.0				
1240	S4	-6489.0	205.0	1300	G326	-7641.0	205.0	1360	G206	-8721.0	205.0	1420	G86	-9801.0	205.0				
1241	S3	-6507.0	340.0	1301	G324	-7659.0	340.0	1361	G204	-8739.0	340.0	1421	G84	-9819.0	340.0				
1242	S2	-6525.0	205.0	1302	G322	-7677.0	205.0	1362	G202	-8757.0	205.0	1422	G82	-9837.0	205.0				
1243	S1	-6543.0	340.0	1303	G320	-7695.0	340.0	1363	G200	-8775.0	340.0	1423	G80	-9855.0	340.0				
1244	TESTO15	-6561.0	205.0	1304	G318	-7713.0	205.0	1364	G198	-8793.0	205.0	1424	G78	-9873.0	205.0				
1245	TESTO16	-6651.0	340.0	1305	G316	-7731.0	340.0	1365	G196	-8811.0	340.0	1425	G76	-9891.0	340.0				
1246	VGLDMY3	-6669.0	205.0	1306	G314	-7749.0	205.0	1366	G194	-8829.0	205.0	1426	G74	-9909.0	205.0				
1247	G432	-6687.0	340.0	1307	G312	-7767.0	340.0	1367	G192	-8847.0	340.0	1427	G72	-9927.0	340.0				
1248	G430	-6705.0	205.0	1308	G310	-7785.0	205.0	1368	G190	-8865.0	205.0	1428	G70	-9945.0	205.0				
1249	G428	-6723.0	340.0	1309	G308	-7803.0	340.0	1369	G188	-8883.0	340.0	1429	G68	-9963.0	340.0				
1250	G426	-6741.0	205.0	1310	G306	-7821.0	205.0	1370	G186	-8901.0	205.0	1430	G66	-9981.0	205.0				
1251	G424	-6759.0	340.0	1311	G304	-7839.0	340.0	1371	G184	-8919.0	340.0	1431	G64	-9999.0	340.0				
1252	G422	-6777.0	205.0	1312	G302	-7857.0	205.0	1372	G182	-8937.0	205.0	1432	G62	-10017.0	205.0				
1253	G420	-6795.0	340.0	1313	G300	-7875.0	340.0	1373	G180	-8955.0	340.0	1433	G60	-10035.0	340.0				
1254	G418	-6813.0	205.0	1314	G298	-7893.0	205.0	1374	G178	-8973.0	205.0	1434	G58	-10053.0	205.0				
1255	G416	-6831.0	340.0	1315	G296	-7911.0	340.0	1375	G176	-8991.0	340.0	1435	G56	-10071.0	340.0				
1256	G414	-6849.0	205.0	1316	G294	-7929.0	205.0	1376	G174	-9009.0	205.0	1436	G54	-10089.0	205.0				
1257	G412	-6867.0	340.0	1317	G292	-7947.0	340.0	1377	G172	-9027.0	340.0	1437	G52	-10107.0	340.0	**Alignment mark**			
1258	G410	-6885.0	205.0	1318	G290	-7965.0	205.0	1378	G170	-9045.0	205.0	1438	G50	-10125.0	205.0		Left	-10655.0	-333.0
1259	G408	-6903.0	340.0	1319	G288	-7983.0	340.0	1379	G168	-9063.0	340.0	1439	G48	-10143.0	340.0		Right	10655.0	-333.0
1260	G406	-6921.0	205.0	1320	G286	-8001.0	205.0	1380	G166	-9081.0	205.0	1440	G46	-10161.0	205.0				

S1 ~ S720 G1 ~ G432 DUMMYR7~10, TESTO11~18 VGLDMY1~4 (No. 300 ~ 1467)	
I/O Pads (No. 1 ~ 299)	

6. Block Description

MPU System Interface

ILI9326 supports three system high-speed interfaces: i80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and serial peripheral interface (SPI). The interface mode is selected by setting the IM[2:0] pins.

ILI9326 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR).

The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9326 read the first data from the internal GRAM. Valid data are read out after the ILI9326 performs the second read operation.

Registers are written consecutively as the register execution time except starting oscillator takes 0 clock cycle.

Registers selection by system interface (8-/9-/16-/18-bit bus width)	I80		
Function	RS	nWR	Nrd
Write an index to IR register	0	0	1
Read an internal status	0	1	0
Write to control registers or the internal GRAM by WDR register.	1	0	1
Read from the internal GRAM by RDR register.	1	1	0

Registers selection by the SPI system interface		
Function	R/W	RS
Write an index to IR register	0	0
Read an internal status	1	0
Write to control registers or the internal GRAM by WDR register.	0	1
Read from the internal GRAM by RDR register.	1	1

Parallel RGB Interface

ILI9326 supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB17-0) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display Interface” section. The ILI9326 allows for switching

between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 233,280 (240 x 432x 18/8) bytes with 18 bits per pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ-correction register to display in 262,144 colors. For details, see the “γ-Correction Register” section.

Timing Controller

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC)

ILI9326 generates RC oscillation with an internal oscillation resistor. The frame rate is adjusted by the register setting.

LCD Driver Circuit

The LCD driver circuit of ILI9326 consists of a 720-output source driver (S1 ~ S720) and a 432-output gate driver (G1~G432). Display pattern data are latched when the 720^{th} bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720 source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Driver Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for driving an LCD.

7. System Interface

7.1. Interface Specifications

ILI9326 has the system interface to read/write the control registers and display graphics memory (GRAM), and the RGB Input Interface for displaying a moving picture. User can select an optimum interface to display the moving or still picture with efficient data transfer. All display data are stored in the GRAM to reduce the data transfer efforts and only the updating data is necessary to be transferred. User can only update a sub-range of GRAM by using the window address function.

ILI9326 also has the RGB interface and VSYNC interface to transfer the display data without flicker the moving picture on the screen. In RGB interface mode, the display data is written into the GRAM through the control signals of ENABLE, VSYNC, HSYNC, DOTCLK and data bus DB[17:0].

In VSYNC interface mode, the internal display timing is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface mode enables to display the moving picture display through the system interface. In this case, there are some constraints of speed and method to write data to the internal RAM.

ILI9326 operates in one of the following 4 modes. The display mode can be switched by the control register. When switching from one mode to another, refer to the sequences mentioned in the sections of RGB and VSYNC interfaces.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM[1:0])
Internal operating clock only (Displaying still pictures)	System interface (RM = 0)	Internal operating clock (DM[1:0] = 00)
RGB interface (1) (Displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM[1:0] = 01)

Note 1) Registers are set only via the system interface.

Note 2) The RGB-I/F and the VSYNC-I/F are not available simultaneously.

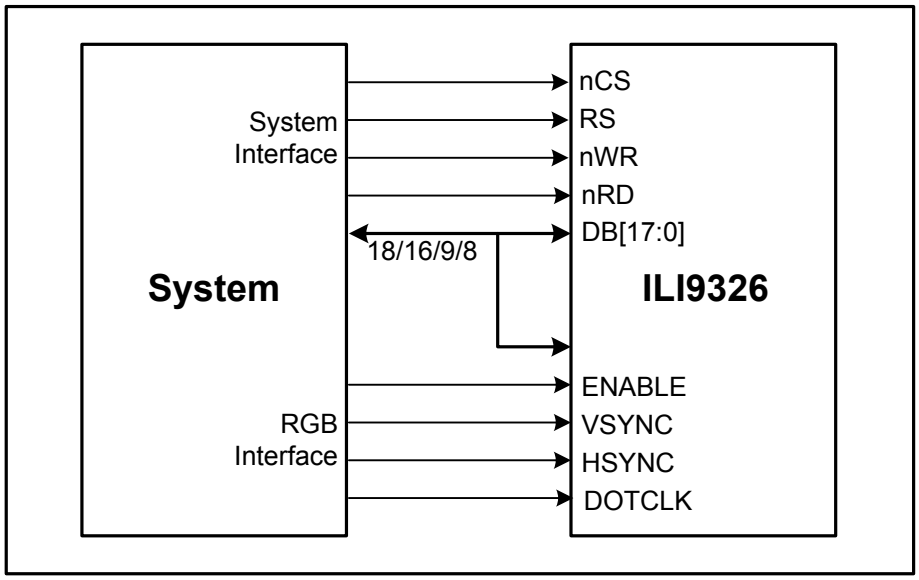


Figure1 System Interface and RGB Interface connection

7.2. Input Interfaces

The following are the system interfaces available with the ILI9326. The interface is selected by setting the IM[2:0] pins. The system interface is used for setting registers and GRAM access.

IM2	IM1	IM0/ID	Interface Mode	DB Pin
0	0	0	i80-system18-bit interface	DB[17:0]
0	0	1	i80-system 9-bit interface	DB[17:9]
0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]
0	1	1	i80-system 8-bit interface	DB[17:10]
1	0	ID	Serial Peripheral Interface (SPI)	SDI, SDO (DB[1:0])
1	1	*	Setting invalid	
1	1	1	MDDI interface	

7.2.1. i80/18-bit System Interface

The i80/18-bit system interface is selected by setting the IM[2:0] as “000” levels.

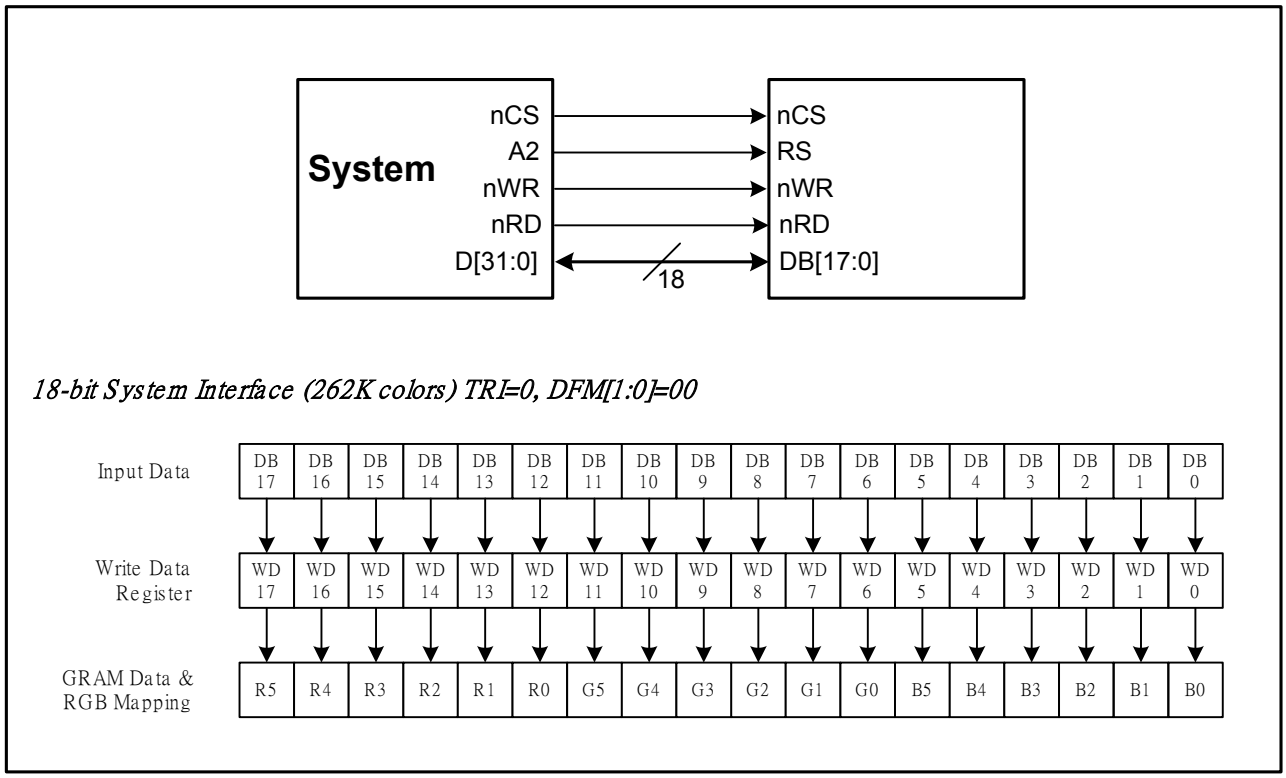


Figure2 18-bit System Interface Data Format

7.2.2. i80/16-bit System Interface

The i80/16-bit system interface is selected by setting the IM[2:0] as “010” levels. The 262K or 65K color can be display through the 16-bit MPU interface. When the 262K color is displayed, two transfers (1st transfer: 2 bits, 2nd transfer: 16 bits or 1st transfer: 16 bits, 2nd transfer: 2 bits) are necessary for the 16-bit CPU interface.

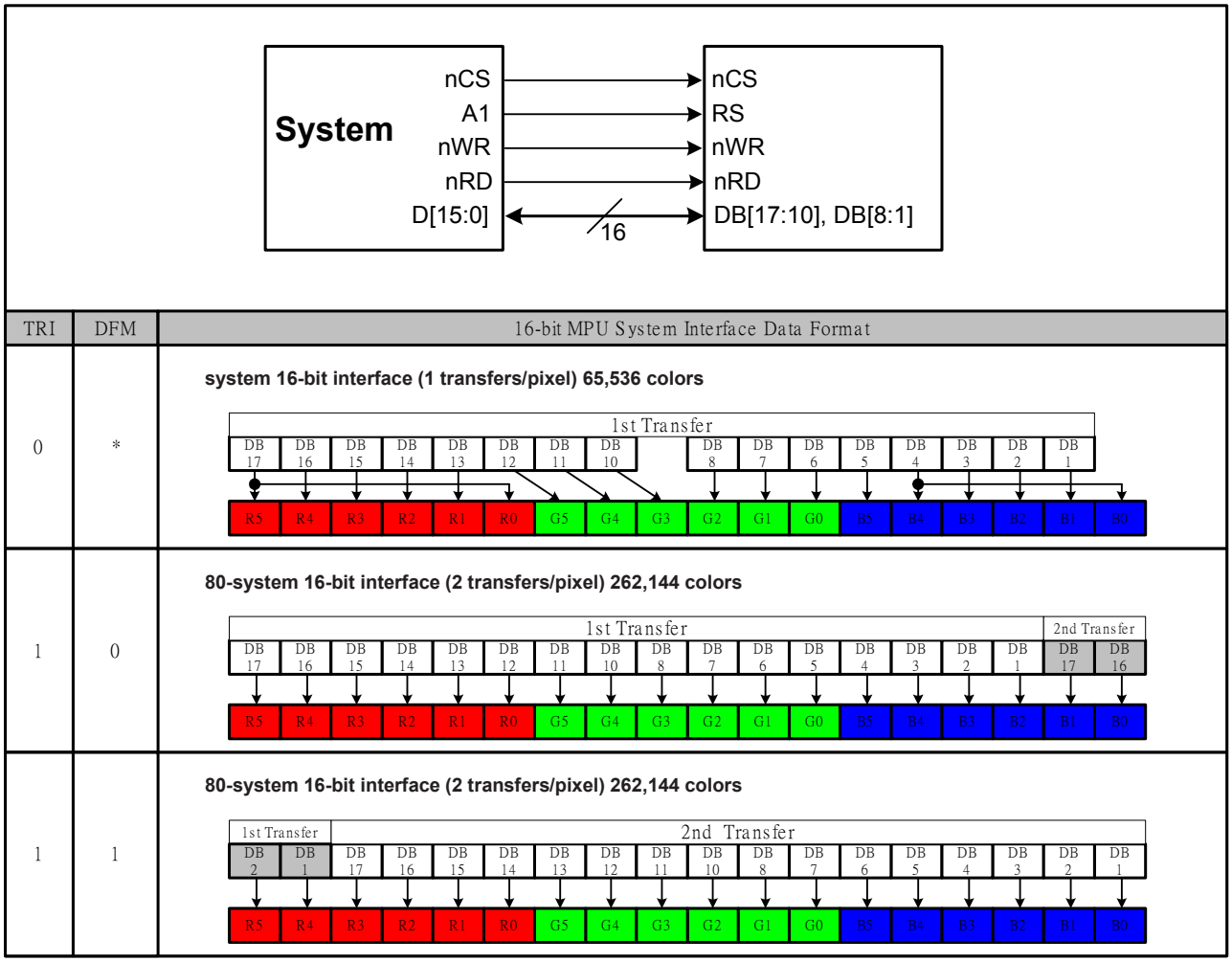


Figure3 16-bit System Interface Data Format

7.2.3. i80/9-bit System Interface

The i80/9-bit system interface is selected by setting the IM[2:0] as “001” and the DB17~DB9 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to either Vcc or AGND.

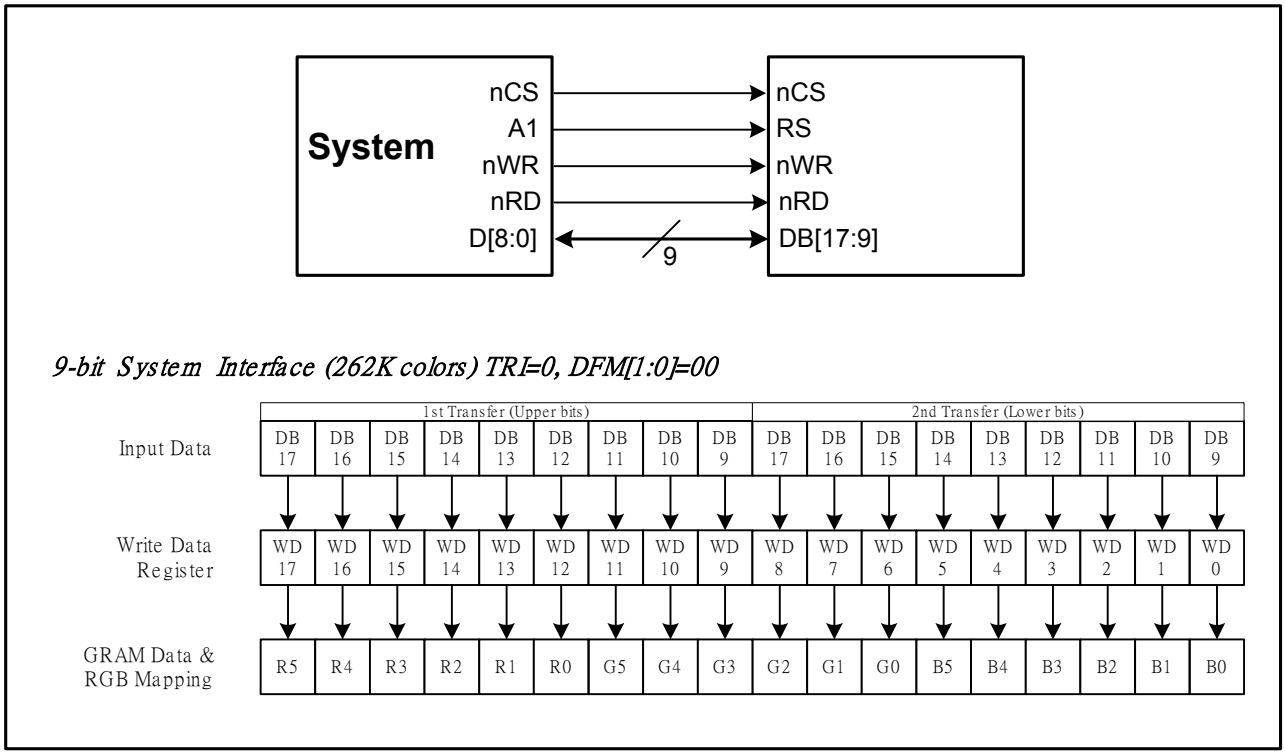


Figure4 9-bit System Interface Data Format

7.2.4. i80/8-bit System Interface

The i80/8-bit system interface is selected by setting the IM[2:0] as “011” and the DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to either Vcc or AGND.

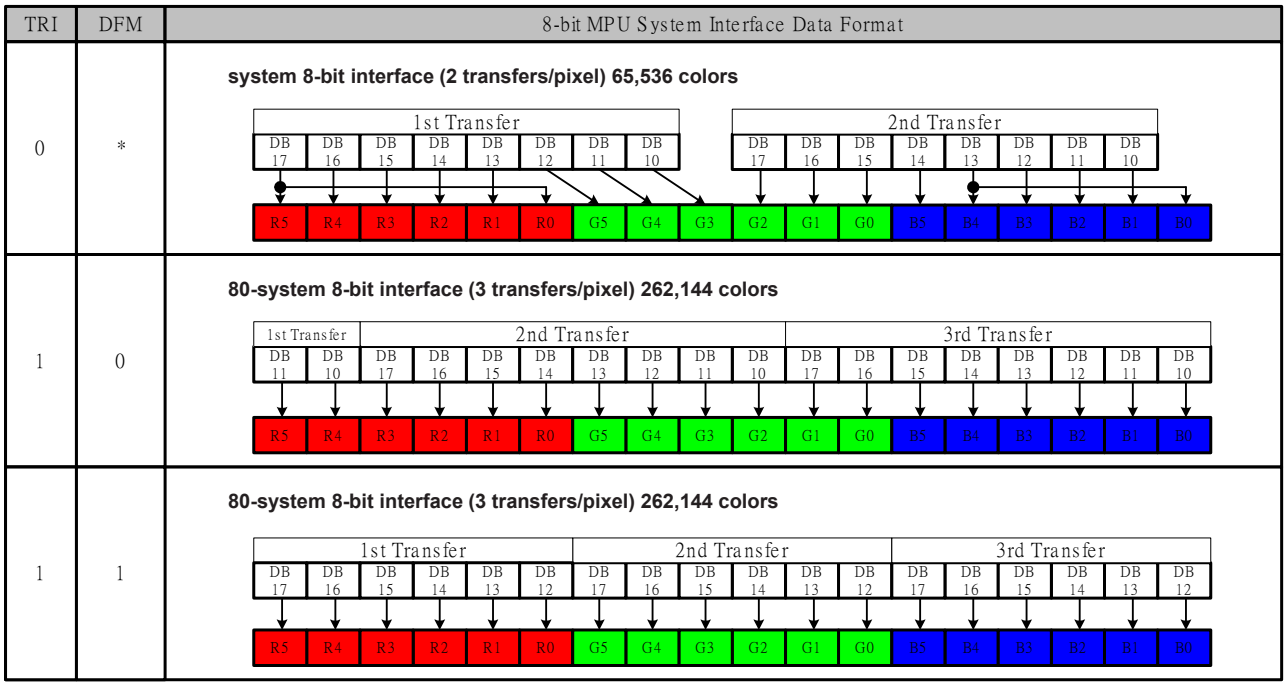


Figure5 8-bit System Interface Data Format

Data transfer synchronization in 8/9-bit bus interface mode

ILI9326 supports a data transfer synchronization function to reset upper and lower counters which count the transfers numbers of upper and lower byte in 8/9-bit interface mode. If a mismatch arises in the numbers of transfers between the upper and lower byte counters due to noise and so on, the “00”h register is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper byte. This synchronization function can effectively prevent display error if the upper/lower counters are periodically reset.

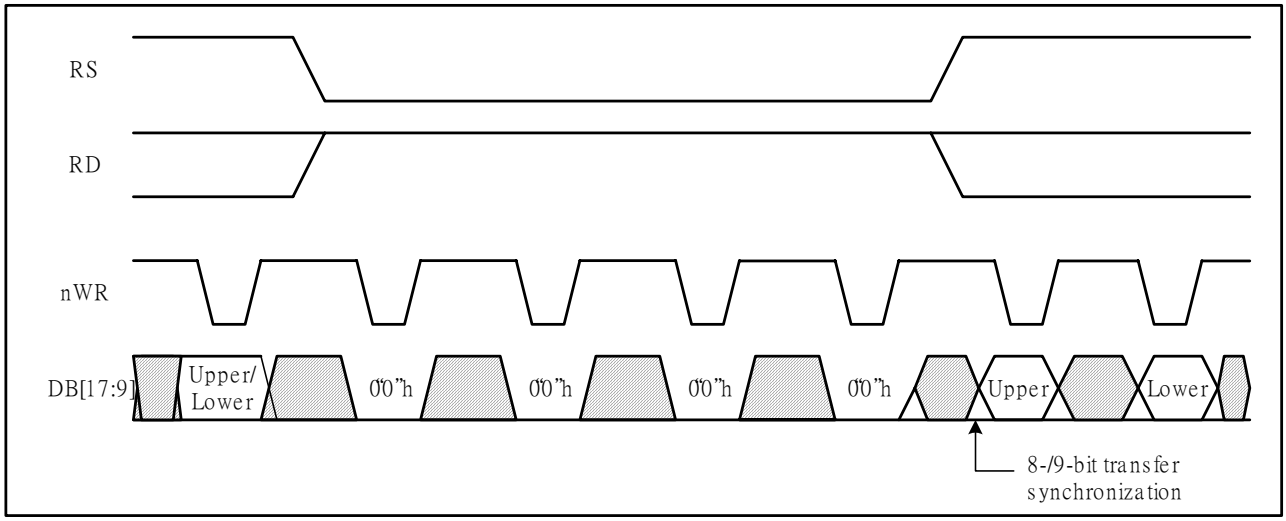


Figure6 Data Transfer Synchronization in 8/9-bit System Interface

7.3. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is selected by setting the IM[2:0] pins as “10x” level. The chip select pin (nCS), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to either IOVCC1 or GND.

The SPI interface operation enables from the falling edge of nCS and ends of data transfer on the rising edge of nCS. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ILI9326.

The seventh bit of start byte is RS bit. When RS = “0”, either index write operation or status read operation is executed. When RS = “1”, either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is “0” and read back when the R/W bit is “1”.

After receiving the start byte, ILI9326 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the ILI9326 are 16-bit format and receive the first and the second byte datat as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID	1/0	1/0

Note: ID bit is selected by setting the IM0/ID pin.

RS and R/W Bit Function

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write a register or GRAM data
1	1	Read a register or GRAM data

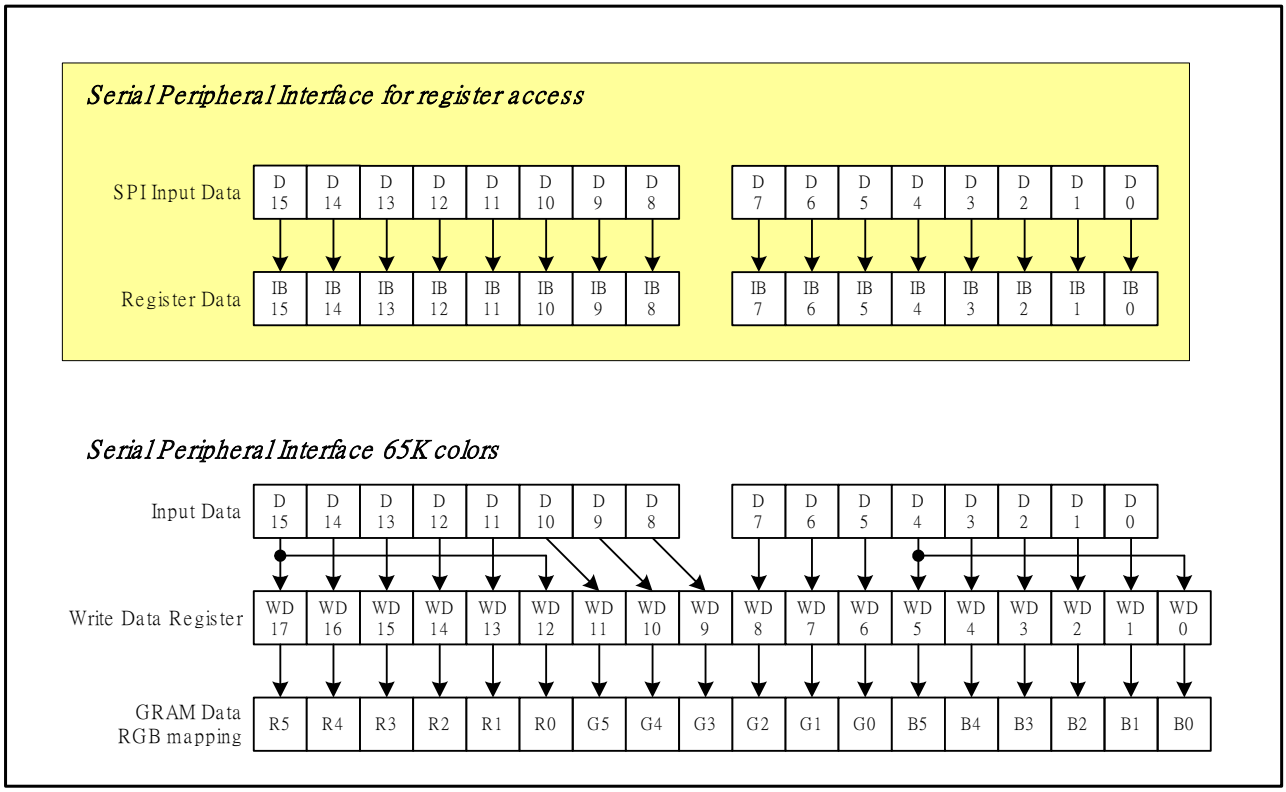


Figure 7 Data Format of SPI Interface

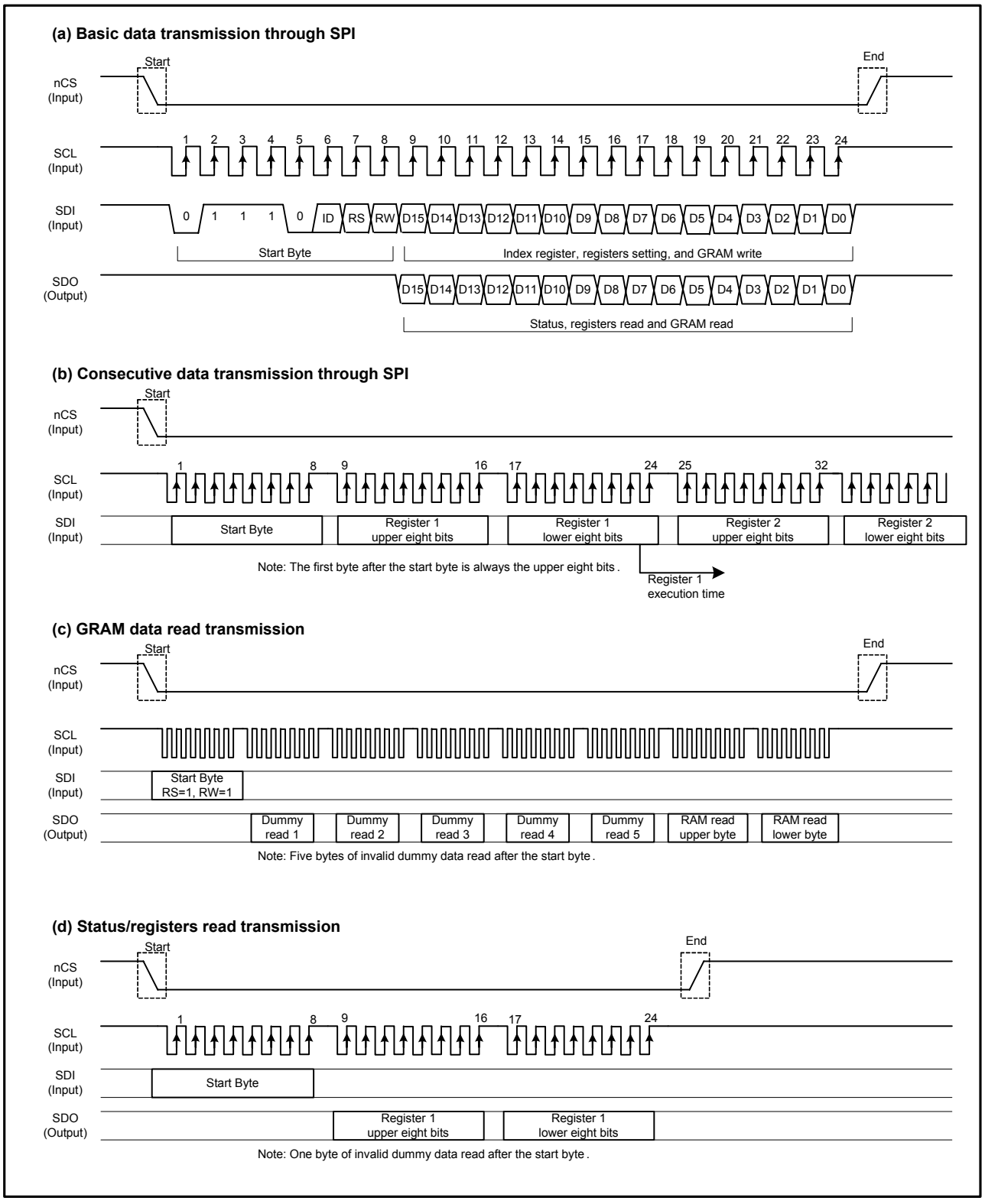
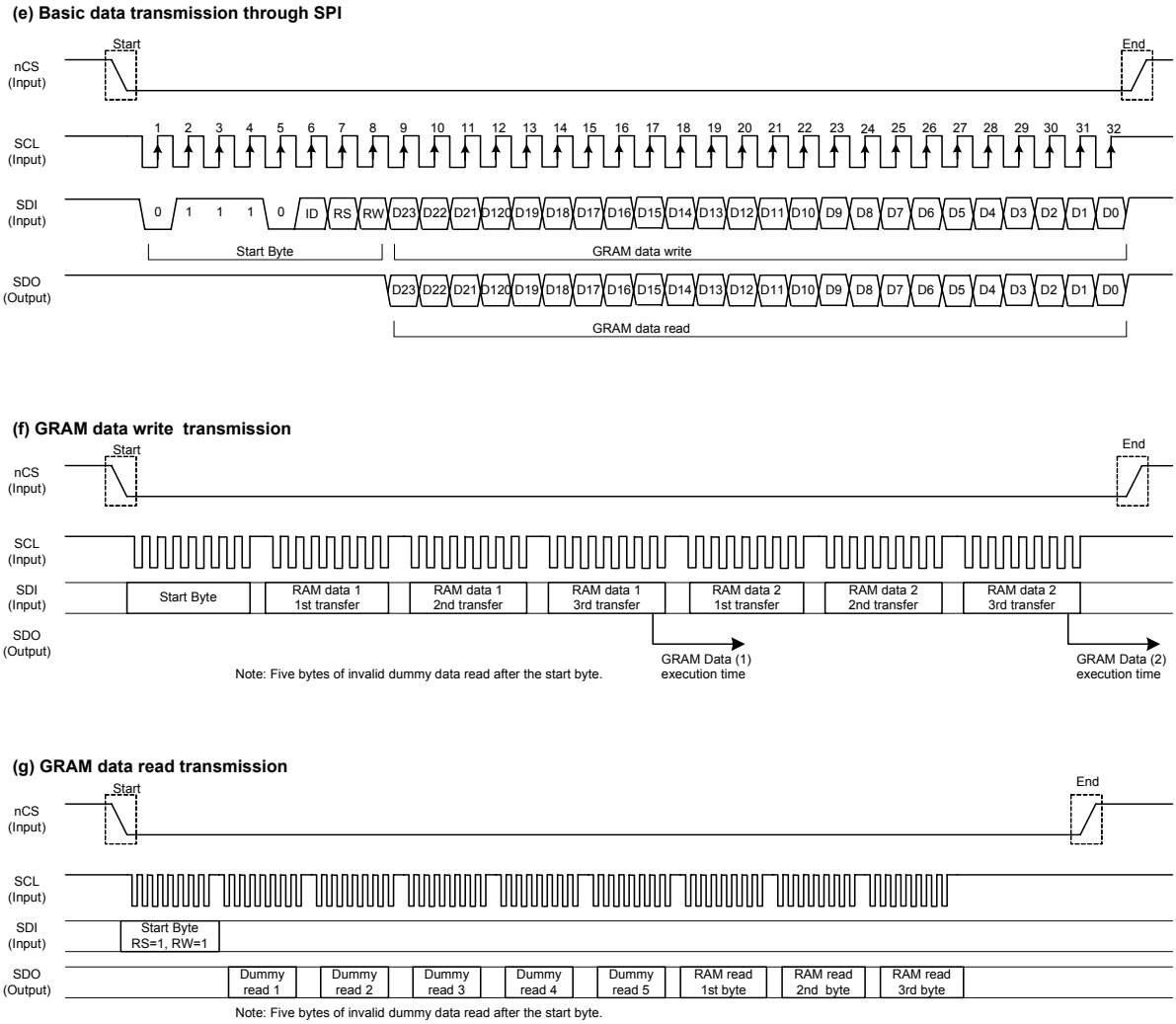


Figure8 Data transmission through serial peripheral interface (SPI)



RAM data transfer in SPI mode when TRI=1 and DFM[1:0]=10.

Figure9 Data transmission through serial peripheral interface (SPI), TRI=”1” and DFM=”10”)

7.4. MDDI (Mobile Display Digital Interface)

MDDI (Mobile display digital interface) is a differential small amplitude serial interface for high-speed data transfer via following 4 lines: Stb+/- (MDDI_STB_P, MDDI_STB_M), Data+/- (MDDI_DATA_P, MDDI_DATA_M).

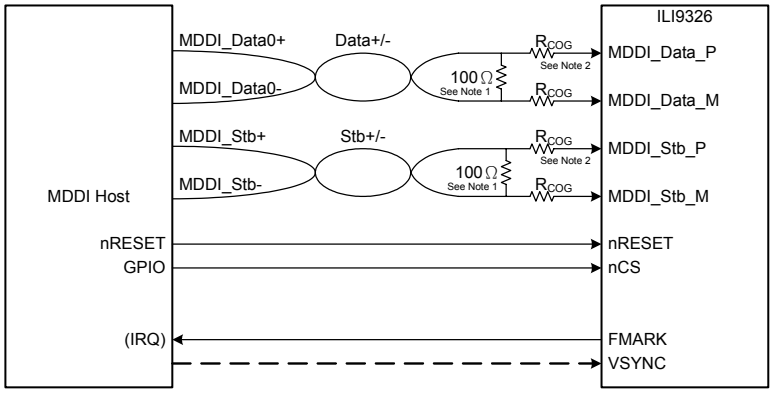
The specifications of MDDI supported by the ILI9326 are compatible to the MDDI specifications disclosed by VESA, Video Electronics Standards Association. The following are the specifications particular to the ILI9326's MDDI.

ILI9326 MDDI Specifications

- MDDI Type-I
- High-speed, differential, small-amplitude data transfer via Stb+/-, Data+/- lines
- MDDI client: the ILI9326 enables direct connection to the base band (BB) chip without bridge chip
- Cost-performance optimized interface for mobile display systems
    1. Only internal mode (one client) and Forward Link are supported
    2. Hibernation mode to save power consumption
    3. Tearing-free moving picture display via FMARK/VSYNC interface
    4. Moving picture display with low power consumption, realized by the features 2 ~ 3
    5. Shutdown mode for saving power consumption in the standby state

Incorporates an output port for sub-display interface or peripheral control

Providing single-chip solution for MDDI mobile display systems



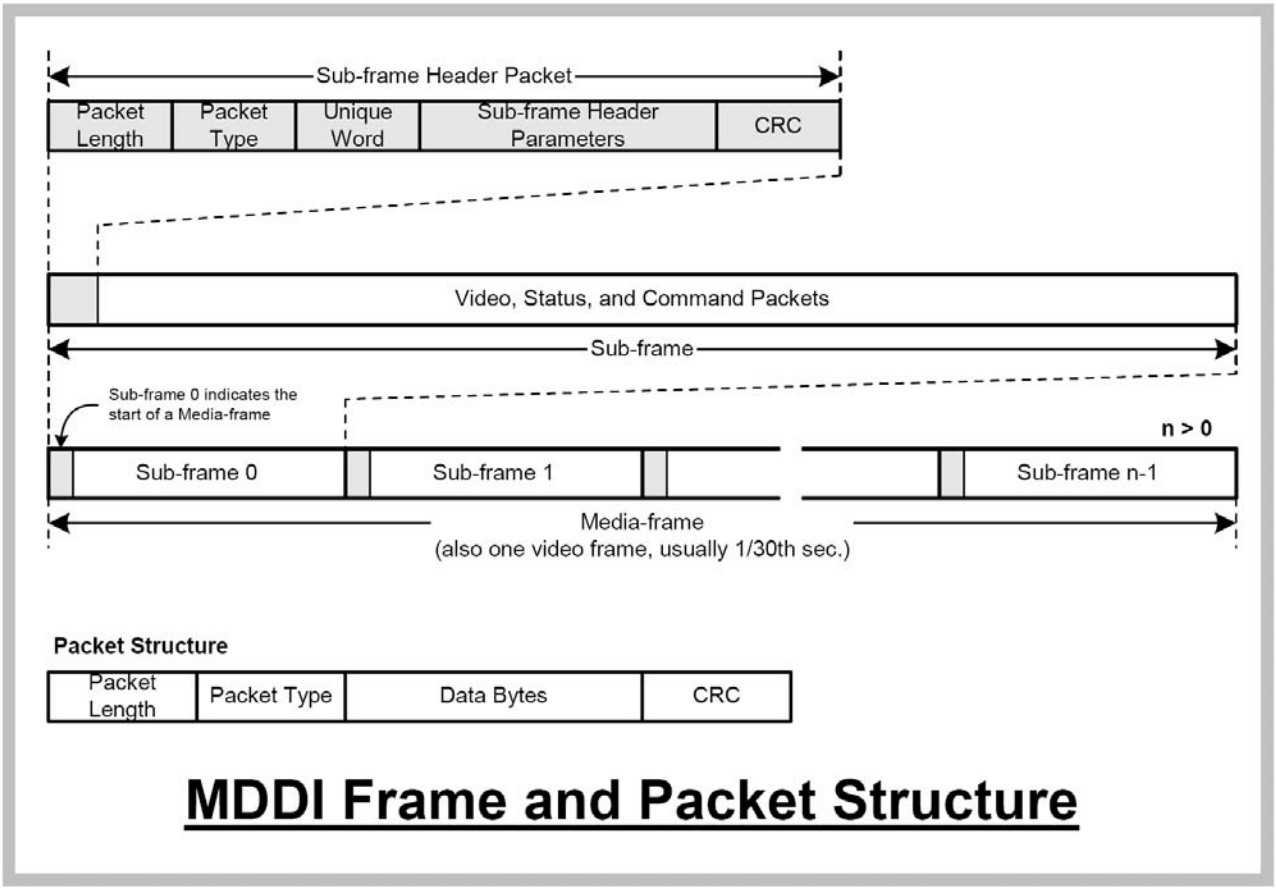
Notes:

1. An external end resistor of 100 ohm is necessary between Data+ and Data- lines
2. Make the COG wiring resistances of Data+/-, Stb+/- lines as small as possible (RCOG < 10 ohm).

MDDI Link Protocol (Packets Supported by the ILI9326)

The MDDI Link Protocol of the ILI9326 is in line with the MDDI specifications disclosed by VESA. See the MDDI specifications by VESA for details on the MDDI Link Protocol.

The MDDI packets supported by the ILI9326 are as follows. Do not send packets not supported by the ILI9326 in the system incorporating the ILI9326.

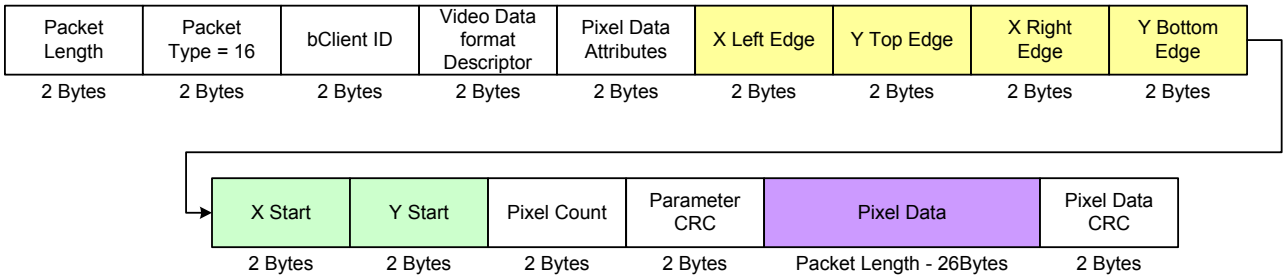


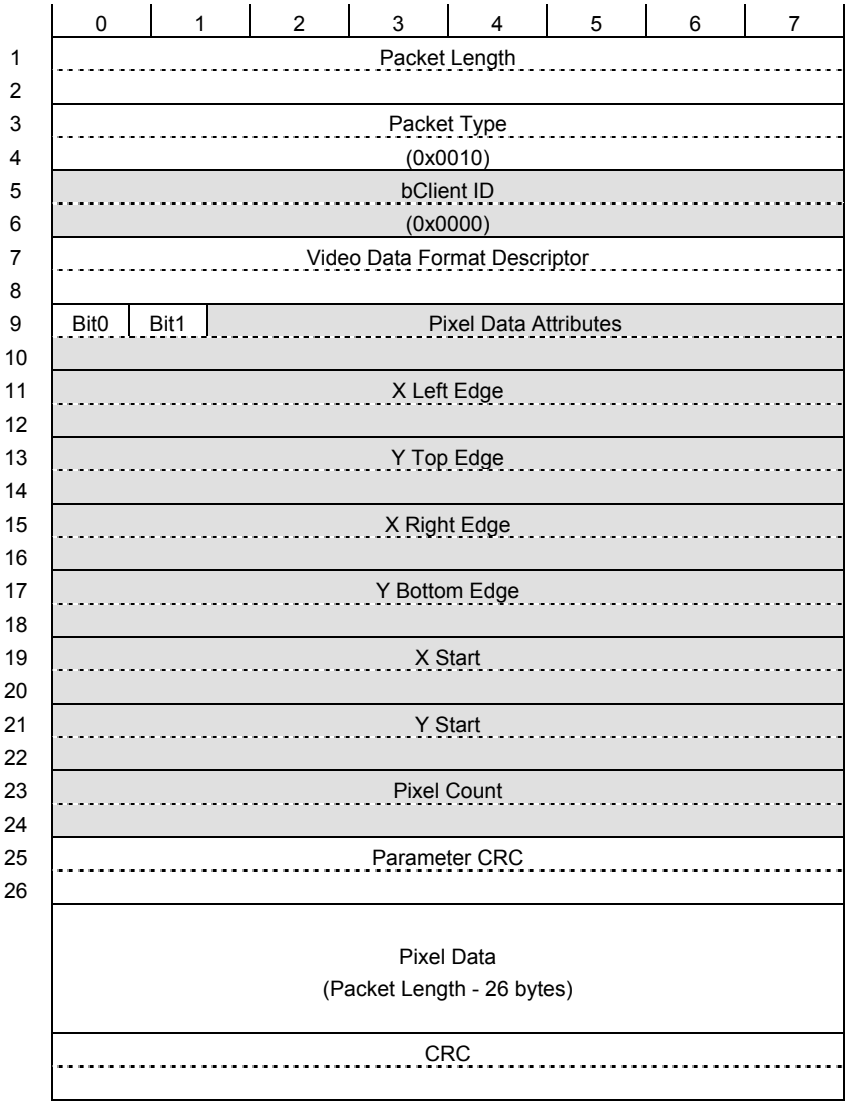
Sub-Frame Header Packet

Bytes	0	1	2	3	4	5	6	7
1	Packet Length							
2	(0x0014)							
3	Packet Type							
4	(0x3bFF)							
5	Unique Word							
6	(0x005A)							
7	Reserved 1							
8	(0x0000)							
9	Sub-Frame Length							
10								
11								
12								
13	Protocol Version							
14	(0x0000)							
15	Sub-frame Count							
16								
17	Media-frame Count							
18	(0x0014)							
19								
20								
21	CRC							
22	(0x0000)							

Video Stream Packet

The ILI9326 writes image data to RAM via Video Stream Packet. The window and RAM addresses are set via Register Access Packet.





Note: The parameters colored in gray are not supported by the ILI9326.

Video Data Format Descriptor: sets the pixel data format. The ILI9326 supports only the following format. Set the same pixel format (bpp) as selected by DSS[1:0] in Video Data Format Descriptor.

[15:13]	[12]	[11:8]	[7:4]	[3:0]	

010	1	0x5	0x6	0x5	Packed 16bpp RGB format (R:G:B=5:6:5)
010	1	0x6	0x6	0x6	Packed 18bpp RGB format (R:G:B=6:6:6)
Others					Setting disabled

	MDDI Bytes n								MDDI Bytes (n+1)								MDDI Bytes (n+2)							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Packet 16bpp	0	1	2	3	4	0	1	2	3	4	5	0	1	2	3	4	0	1	2	3	4	0	1	2
	Pixel 1 Blue					Pixel 1 Green						Pixel 1 Red					Pixel 2 Blue					Pixel 2		
Packet 18bpp	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5
	Pixel 2 Blue						Pixel 2 Green						Pixel 2 Red				Pixel 2 Blue							

Pixel Data Attributes: the image data sent vial Video Stream Packet is recognized as either the data for the main-panel or for the sub-panel according to the setting in [1:0] bits in this field.

Pixel Data Attributes	Bits[1:0]	Description
0x0000	00	***ILI9326 doesn't support the sub-panel display.***
0x0001	01	Setting disabled
0x0002	10	
0x0003	11	The Video Stream Packet data is recognized as the data written in the ILI9326. The Video Stream Packet data is written in the ILI9326 and not outputted via sub-display interface.
Others		

Register Access Packet

Register Access Packet is used when setting instruction to the ILI9326. Do not use this packet for RAM access.

	0	1	2	3	4	5	6	7
1	Packet Length							
2								
3	Packet Type							
4	(0x0092)							
5	bClient ID							
6	(0x0000)							
7	Read/Write Info.							
8								
9	Register Address							
10								
11								
12								
13	Parameter CRC							
14								
	Pixel Data (Packet Length - 14 bytes)							
	Register Dara CRC							

Note: The parameters colored in gray are not supported by the ILI9326.

Read/Write Info: Read or Write information in register access. The ILI9326 supports only the following access setting

Bits[15:14]	Bits[13:0]	Function
00	0x0001	Single Access mode, in which one instruction is set via one register access packet
00	0xn	In multi random access mode, the number of Register Data (index+instruction) is set.
Others		Setting disabled.

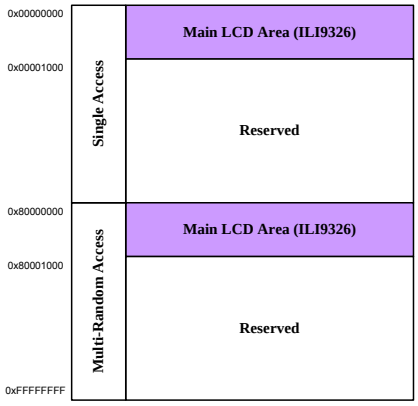
Register Address

The index of the register to be accessed is set in Register Address area. Also, the register access mode, i.e. single or multi random access mode, and whether the Register Address Packet is directed to the ILI9326 or the sub display are determined by the setting in Register Address area.

Bits[31]	Description
0	Single Access mode. The index of the register to be accessed (ID[11:0]) is set in bits[11:0] in Register Address. The instruction set (IB[15:0]) to be written in the register is stored in the Register Data area in Register Access Packet.
1	Multi Random Access mode. The index of the register to be accessed (ID[11:0]) is stored in the upper 2 bytes in the Register Data area in Register Access Packet. The instruction set (IB[15:0]) to be written in the register is stored in the lower 2 bytes in the Register Data area in Register Access Packet. In Multi Random Access mode, both index and instruction set are stored in the Register Data area and instruction set can be transferred consecutively without setting the index in Register Address in each time transferring instruction.

Bits[30:12]	Description
19'h00000	The Register Access Packet is directed to the ILI9326 via main-display interface.
19'h00001	The Register Access Packet is directed to the sub display via sub-display interface.
19'h00002 ~ 19'h7FFFF	Setting disabled

Bits[11:0]	Description
Single Access	Bits [11:0] are used as index [11:0].
Multi Random Access	In Multi Random Access mode, bits [11:0] are not used. Set "0" to all bits.



Register Data

The data for register access is written in Register Data. Four bytes are allocated for one instruction.

Bits[31:16]	Bits[15:0]	Description
All 0	Instruction IB[15:0]	In Single access mode, the instruction set written in bits[15:0] is set in the register, which is specified in the bits[11:0] in Register Address.
4h0 + IndexID[11:0]	Instruction IB[15:0]	In Multi Random Access mode, both index and instruction set are stored in Register Data to allow consecutive instruction setting without setting the index in Register Address in each time transferring instruction.

Example of Register Access Packet in Single Access mode (e.g. write to the ILI9326)

	0	1	2	3	4	5	6	7
1	Packet Length							(0x12)
2								(0x00)
3	Packet Type							(0x92)
4								(0x00)
5	bClient ID							(0x00)
6								(0x00)
7	Read/Write Info.							(0x01)
8								(0x00)
9	Register Address							(index ID[7:0])
10								(0x0, upper index ID[11:8])
11								(0x00)
12								(0x00)
13	Parameter CRC							
14								
15	Register Data List							(lower instruction IB[7:0])
16								(Upper instruction IB[15:8])
17								(0x00)
18								(0x00)
19	Parameter CRC							
20								

Note: The parameters colored in gray are not supported by the ILI9326.

Example of Register Access Packet in Multi Random Access mode (e.g. write 4 instructions to the ILI9326)

	0	1	2	3	4	5	6	7
1	Packet Length						(0x1E)	
2							(0x00)	
3	Packet Type						(0x92)	
4							(0x00)	
5	bClient ID						(0x00)	
6							(0x00)	
7	Read/Write Info.						(0x04)	
8							(0x00)	
9	Register Address						(0x00)	
10							(0x00)	
11							(0x00)	
12							(0x80)	
13	Parameter CRC							
14								
15	Register Data List 1st index + instruction					(Lower instruction IB1[7:0])		
16						(Upper instruction IB1[15:8)		
17						(Lower Index ID1[7:0])		
18						(Upper indexID1[15:8)		
19	Register Data List 2nd index + instruction					(Lower instruction IB2[7:0])		
20						(Upper instruction IB2[15:8)		
21						(Lower Index ID2 [7:0])		
22						(Upper indexID2 [15:8)		
23	Register Data List 3rd index + instruction					(Lower instruction IB3[7:0])		
24						(Upper instruction IB3[15:8)		
25						(Lower Index ID3 [7:0])		
26						(Upper indexID3[15:8)		
27	Register Data List 4th index + instruction					(Lower instruction IB4[7:0])		
28						(Upper instruction IB4[15:8)		
29						(Lower Index ID4[7:0])		
30						(Upper indexID4[15:8)		
31	Parameter CRC							
32								

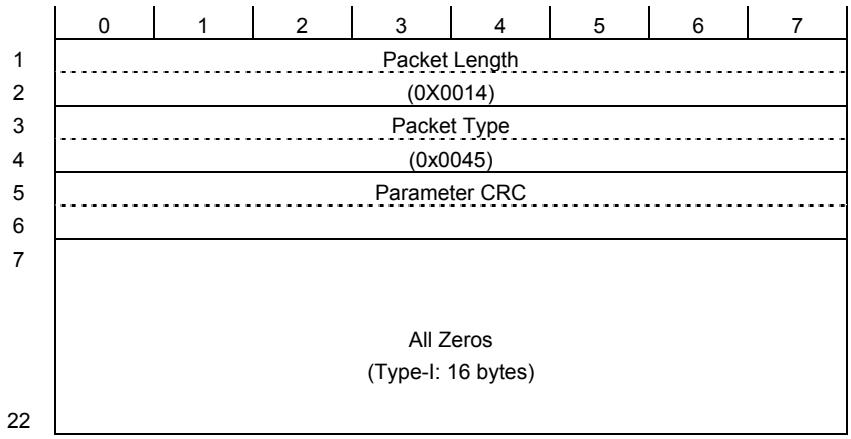
Note: The parameters colored in gray are not supported by the ILI9326.

Register Access Packet Restrictions

The ILI9326's internal RAM is accessible via Video Stream Packet. RAM access data is not included in Register Access Packet.

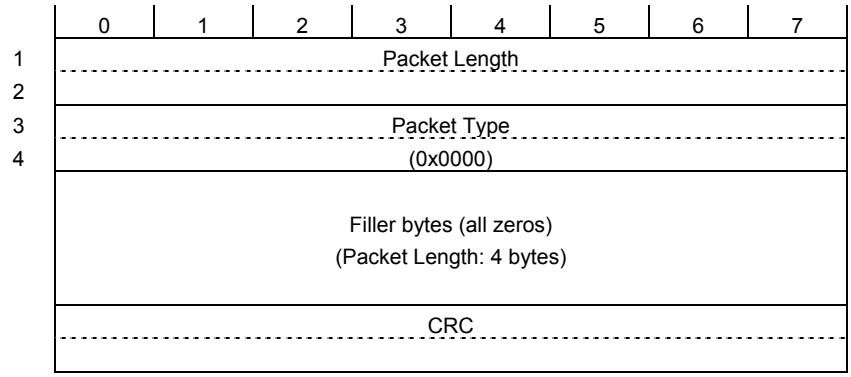
Link Shutdown Packet

This packet is used to bring Link to the Hibernation state.



Note: The parameters colored in gray are not supported by the ILI9326.

Filler Packet



MDDI Instruction Setting

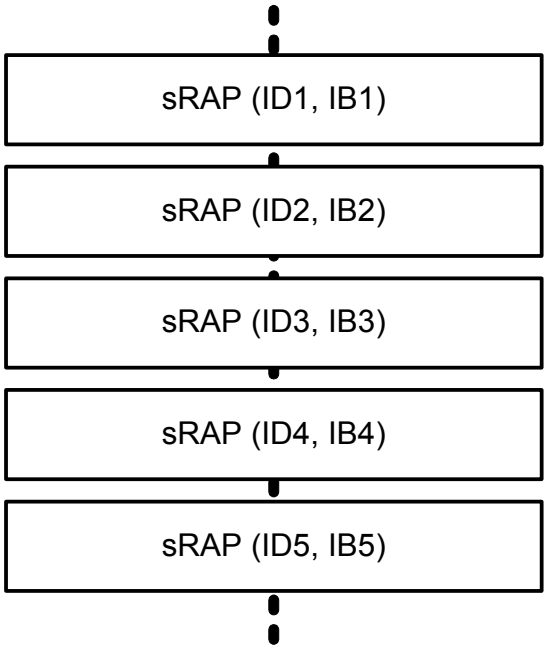
Instruction Setting in Single Access Mode

In Single Access mode, one instruction set is transferred in one Register Access Packet. When transferring multiple numbers of instruction sets, they must be transferred in the same number of Register Access Packets.

Register Access Packet Parameter	Register Setting
Read/Write Info[15:0]	0x0001
Register Address[31:0]	20'h0000000+ID[11:0]
Register Data[31:0]	16'h0000+IB[15:0]

MDDI Packet

sRAP(x,y) = Single Register Access Packet (ID[15:0], IB[15:0])



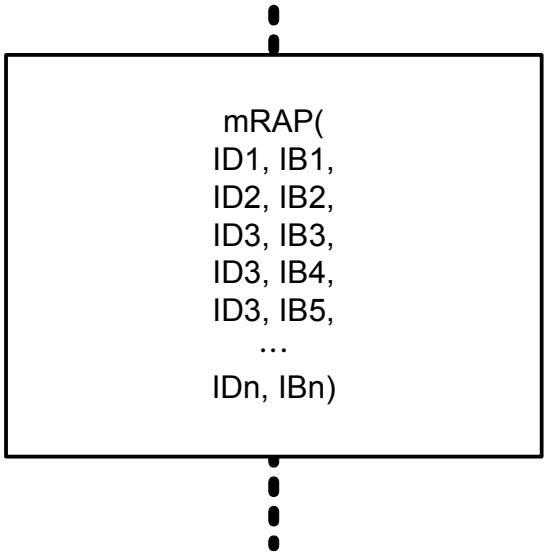
Instruction Setting via Multi Random Access Mode

In Multi Random Register Access operation, both index and instruction set are stored in one field of Register Data List in the Register Access Packet to allow random instruction setting. In this mode, a multiple number of instruction sets can be transferred in one Register Access Packet.

Register Access Packet Parameter	Register Setting
Read/Write Info [15:0]	0 x n (n: Number of Register List)
Register Address [31:0]	32'h8000_0000
Register Data List [31:0]	ID[15:0]+IB[15:0]

MDDI Packet

sRAP(x,y) = Multi-random Register Access Packet (ID[15:0], IB[15:0])



RAM Access Setting Example

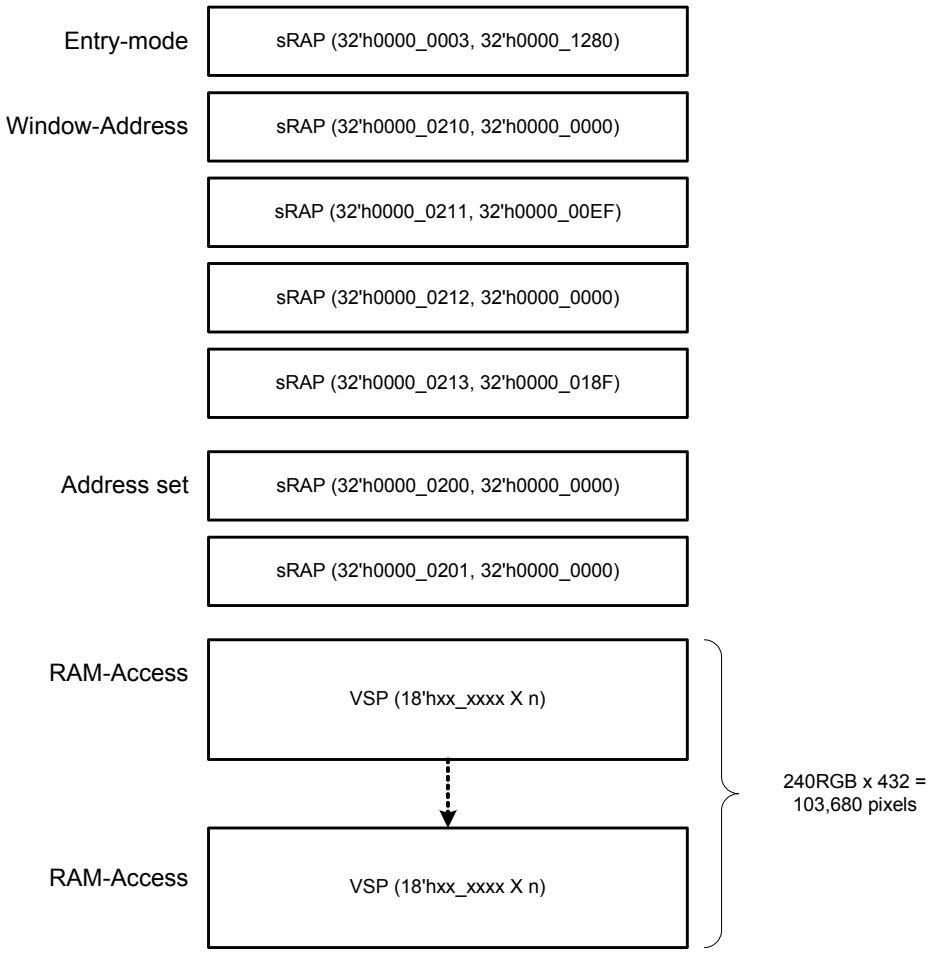
The following are examples of RAM access via Video Stream Packet and register access via Register Access Packet in Single and Multi Random Access modes.

Example: 240RGB x 432 panel, full screen rewrite, 18bpp data

MDDI Packet: Single Access Mode

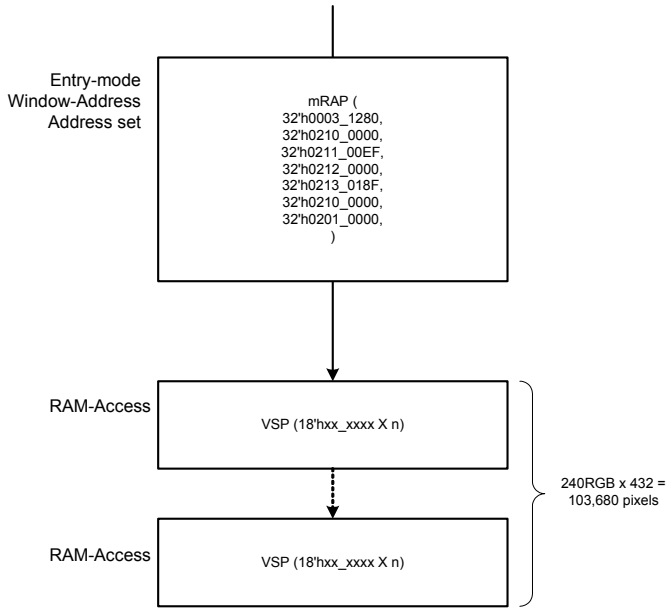
sRAP (x, y) = Register Access Packet (ID[15:0], IB[15:0]) in Single Access Mode

VSP (p, n) = Video Stream Packet (pixel data)



MDDI Packet: Multi Random Access Mode

mRAP (x, y) = Register Access Packet (ID[15:0], IB[15:0]) in Multi Random Access mode. VSP (p, n) = Video Stream Packet (pixel data)



Video Stream Access Packet Restriction	
AM	0 (Horizontal write)
HWM	1 (High-speed write)
Data write transfer to RAM	Transfer data for each line at a time within the window address area.
RAM start address RAM window address	Set them via register access packet

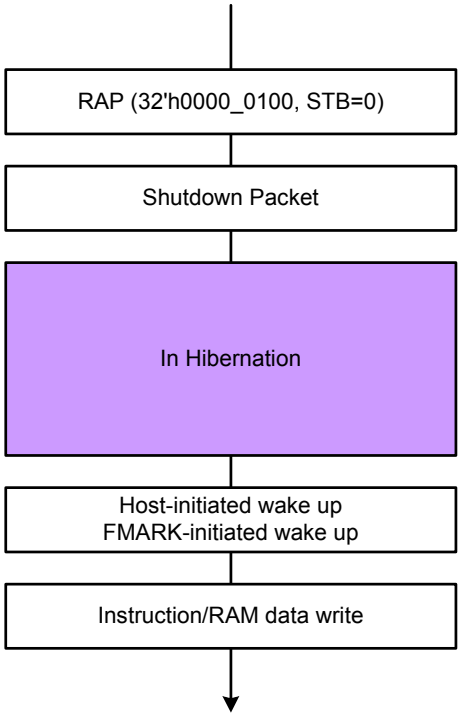
Register Packet Restriction	
RAM access	The ILI9326's internal RAM is accessible via Video Stream Packet. RAM access data is not included in Register Access Packet.

Hibernation Setting

The ILI9326's Client MDDI supports Hibernation setting. There are two ways to cancel the Hibernation setting, which can be selected according to the condition of use.

Hibernation Cancellation	
Host-initiated wake up	In power-saving mode such as standby
FMARK-initiated wake up	Save power consumption in transferring moving picture data Host-initiated wake up triggered by the output from FMARK.

The Hibernation setting and cancellation sequence must be compatible with the VESA-MDDI specifications.

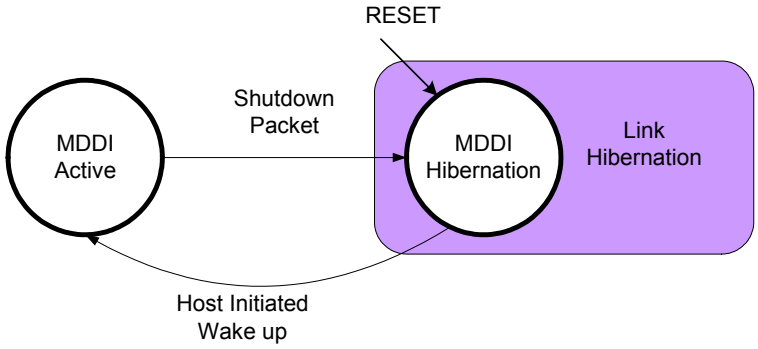


Shutdown Mode Setting

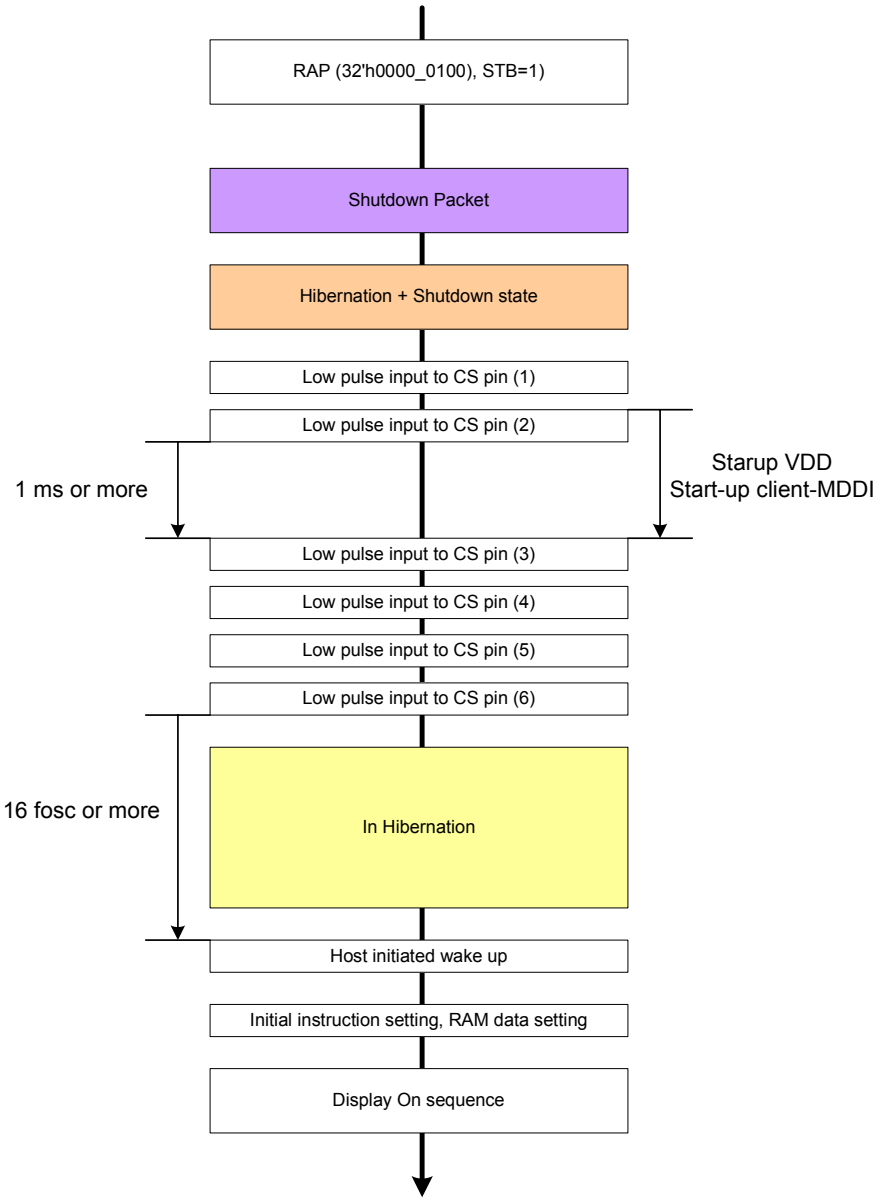
The ILI9326's Client MDDI supports shutdown setting to bring the ILI9326 to the standby state to save power consumption during Hibernation.

By setting STB = 1 and sending Shutdown Packet, MDDI enters the Hibernation state. The Client MDDI's standby power requirement can be reduced while MDDI Link is maintained in the Hibernation state. In shutdown mode, the ILI9326 halts operation other than maintaining Hibernation state. In canceling shutdown mode, input Low pulse 6 times from CS pin. After canceling shutdown mode, cancel the Hibernation state by Host-initiated Wake up. In shutdown mode, instruction setting and RAM data are not retained and they must be reset after canceling the Hibernation state.

When setting and canceling the Hibernation state, follow the sequence as specified in the MDDI specifications by VESA.



Shutdown Mode Sequence



Note: In MDDI operation, the CS pin is used only for cancelingthe shutdown mode.

7.5. VSYNC Interface

ILI9326 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the i80 system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = “10” and RM = “0”.

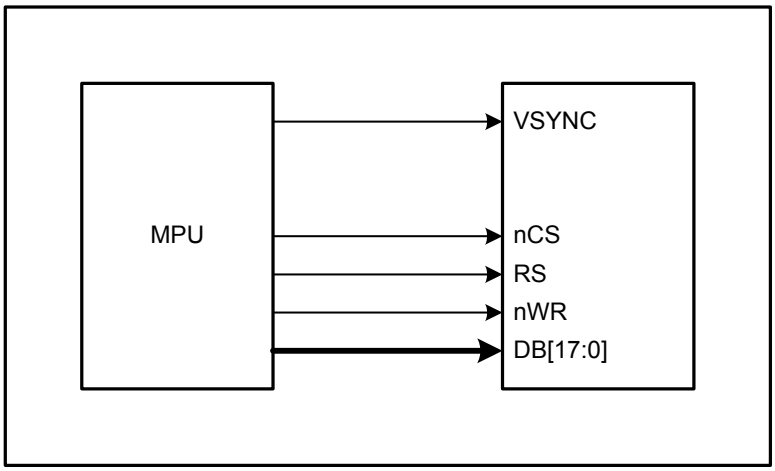


Figure10 Data transmission through VSYNC interface)

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

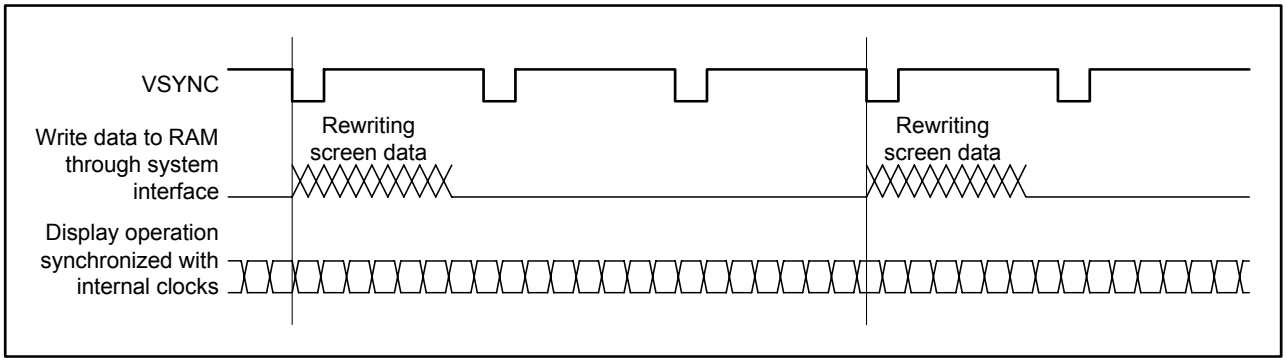


Figure11 Moving picture data transmission through VSYNC interface

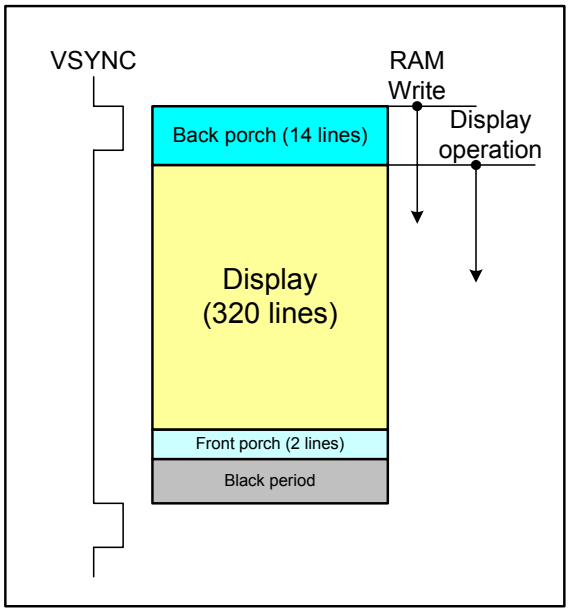


Figure12 Operation through VSYNC Interface

The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (FP) + BackPorch (BP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\textit{Minimum RAM write speed (HZ)} > \frac{\textit{240 x DisplayLines (NL)}}{\textit{[(BackPorch(BP)+DisplayLines(NL) - margins] x 16 (clocks) x 1/fosc}}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 240 RGB × 432 lines

Lines: 432 lines (NL = 110101)

Back porch: 14 lines (BP = 1110)

Front porch: 2 lines (FP = 0010)

Frame frequency: 60 Hz

Frequency fluctuation: 10%

Internal oscillator clock (fosc.) [Hz] = 60 x [432+ 2 + 14] x 16 clocks x (1.1/0.9) ≒ 394KHz

When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz] > 240 x 432 x 394K / [(14 + 432 – 2)lines x 16clocks] ≒ 5.7 MHz

The above theoretical value is calculated based on the premise that the ILI9326 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 5.7MHz or more will guarantee the completion of GRAM write operation before the ILI9326 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode and set the AM bit to “0” to transfer display data.

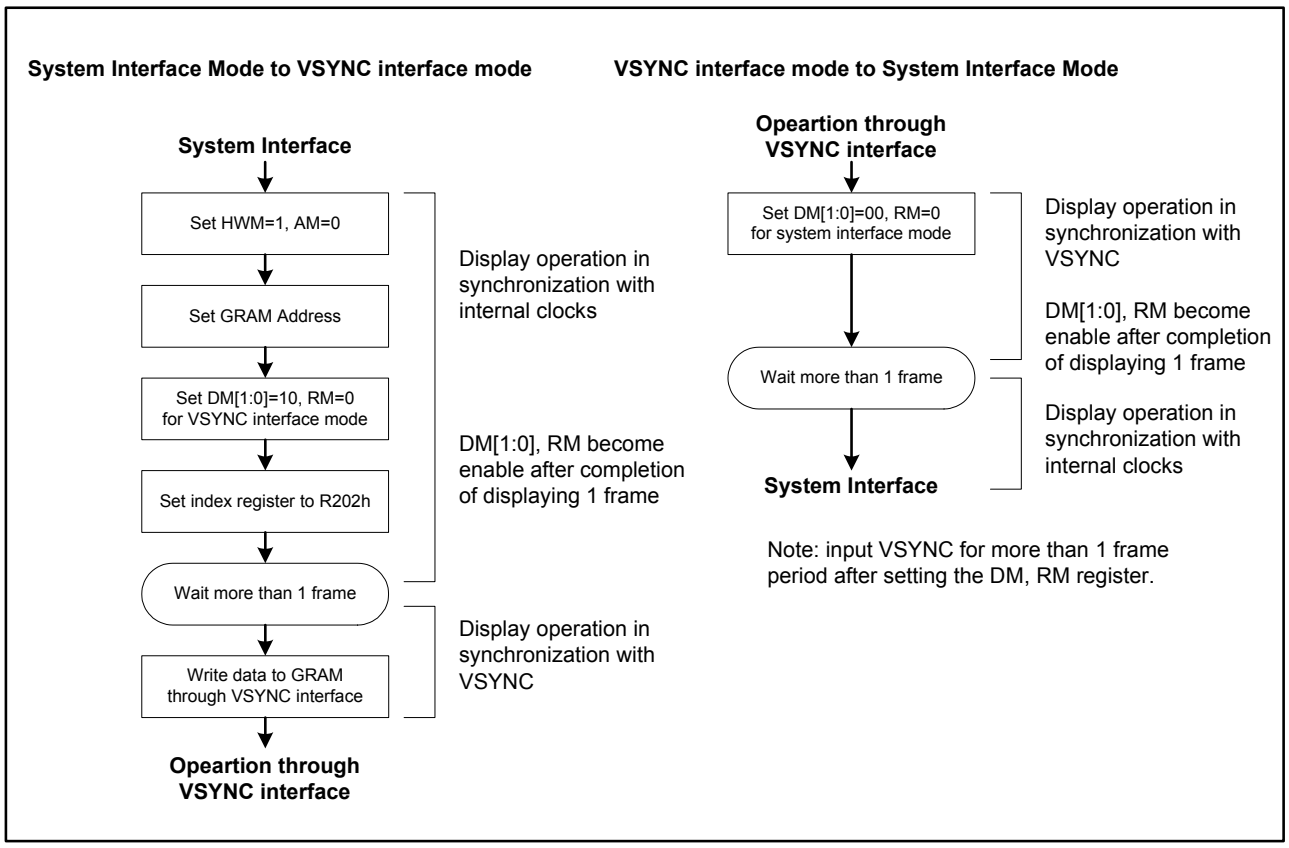


Figure13 Transition flow between VSYNC and internal clock operation modes

7.6. RGB Input Interface

The RGB Interface mode is available for ILI9326 and the interface is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface	DB pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	

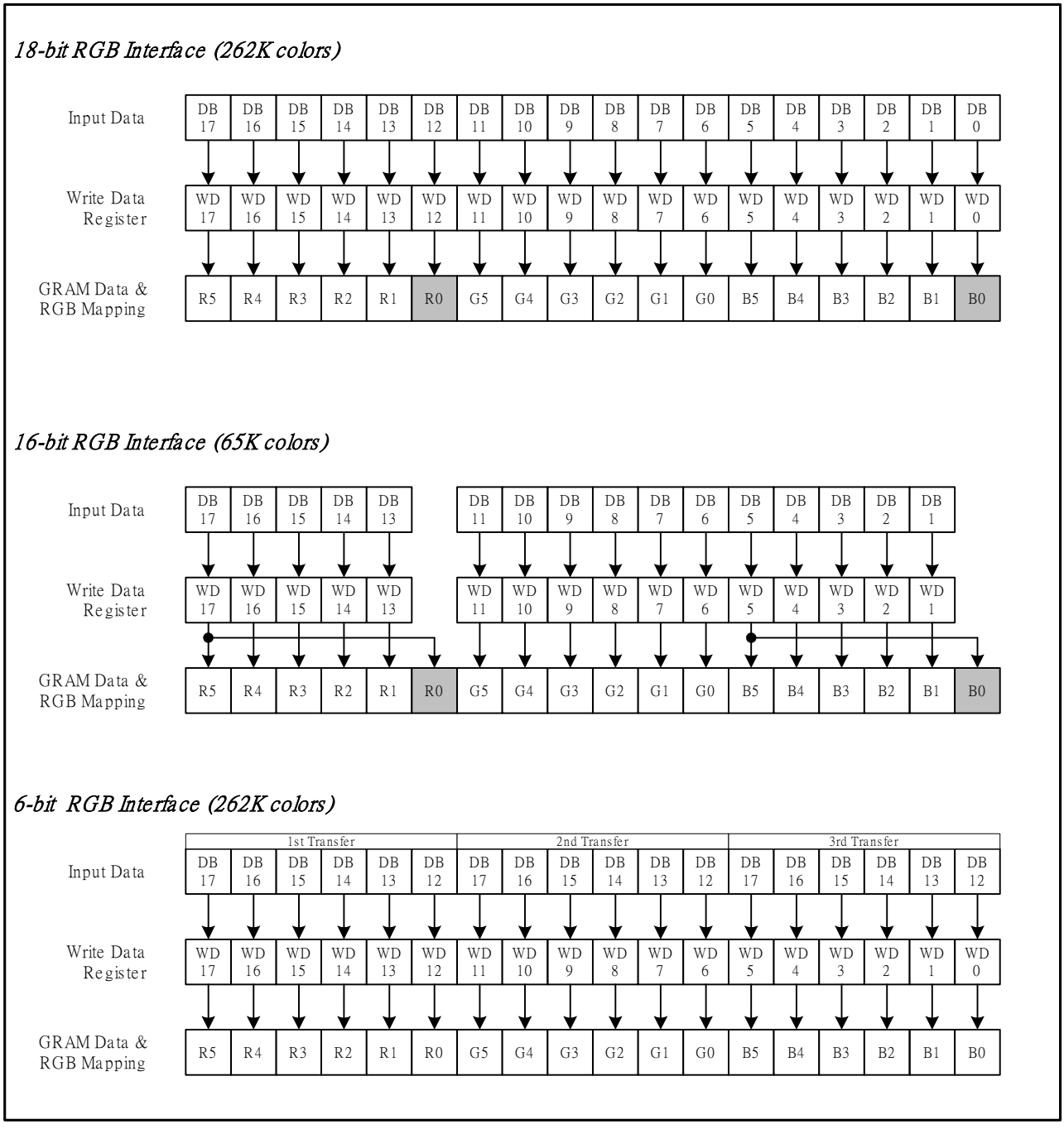


Figure14 RGB Interface Data Format

7.6.1. RGB Interface

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The RGB interface transfers the updated data to GRAM with the high-speed write function and the update area is defined by the window address function. The back porch and front porch are used to set the RGB interface timing.

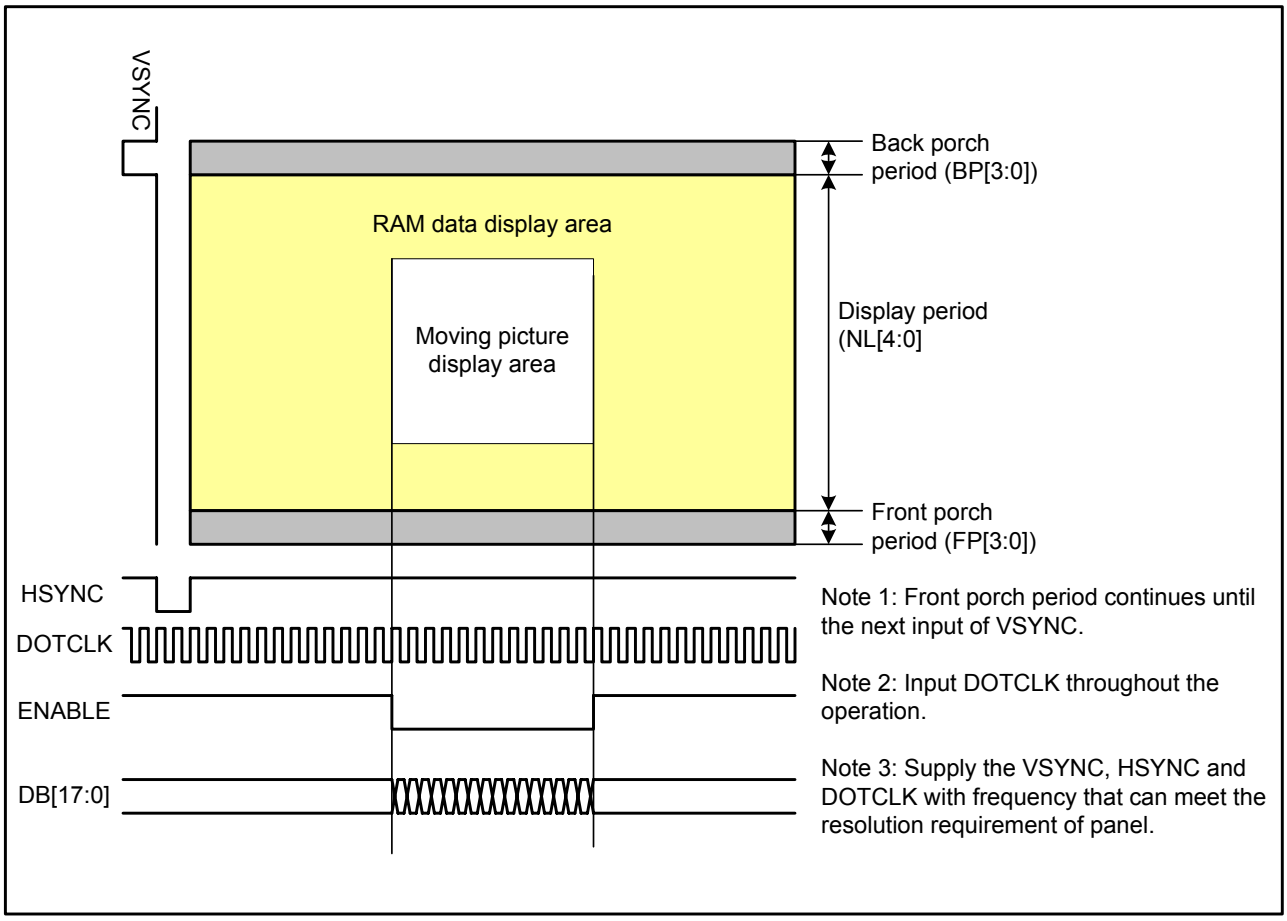


Figure15 GRAM Access Area by RGB Interface

7.6.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as follows.

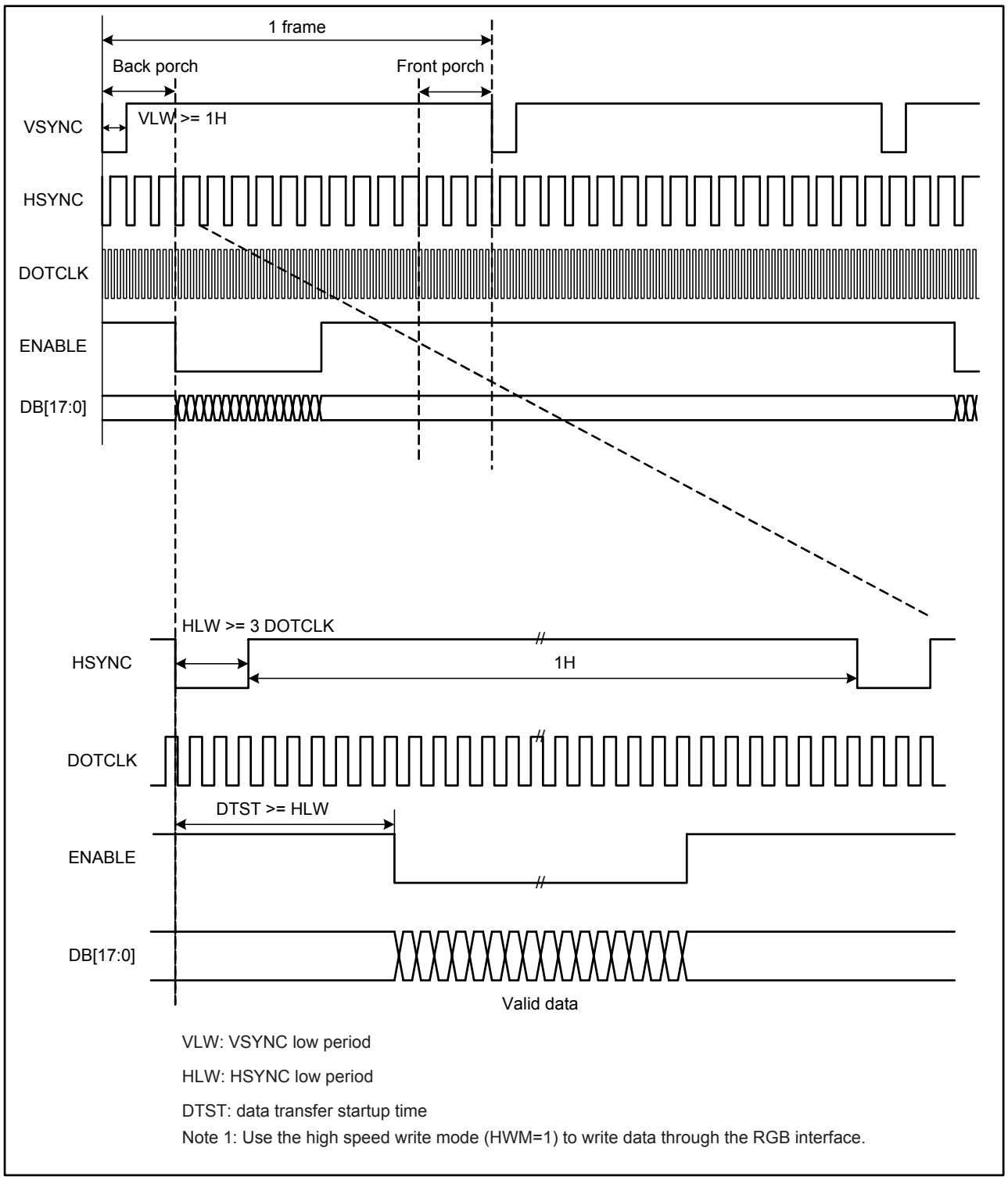
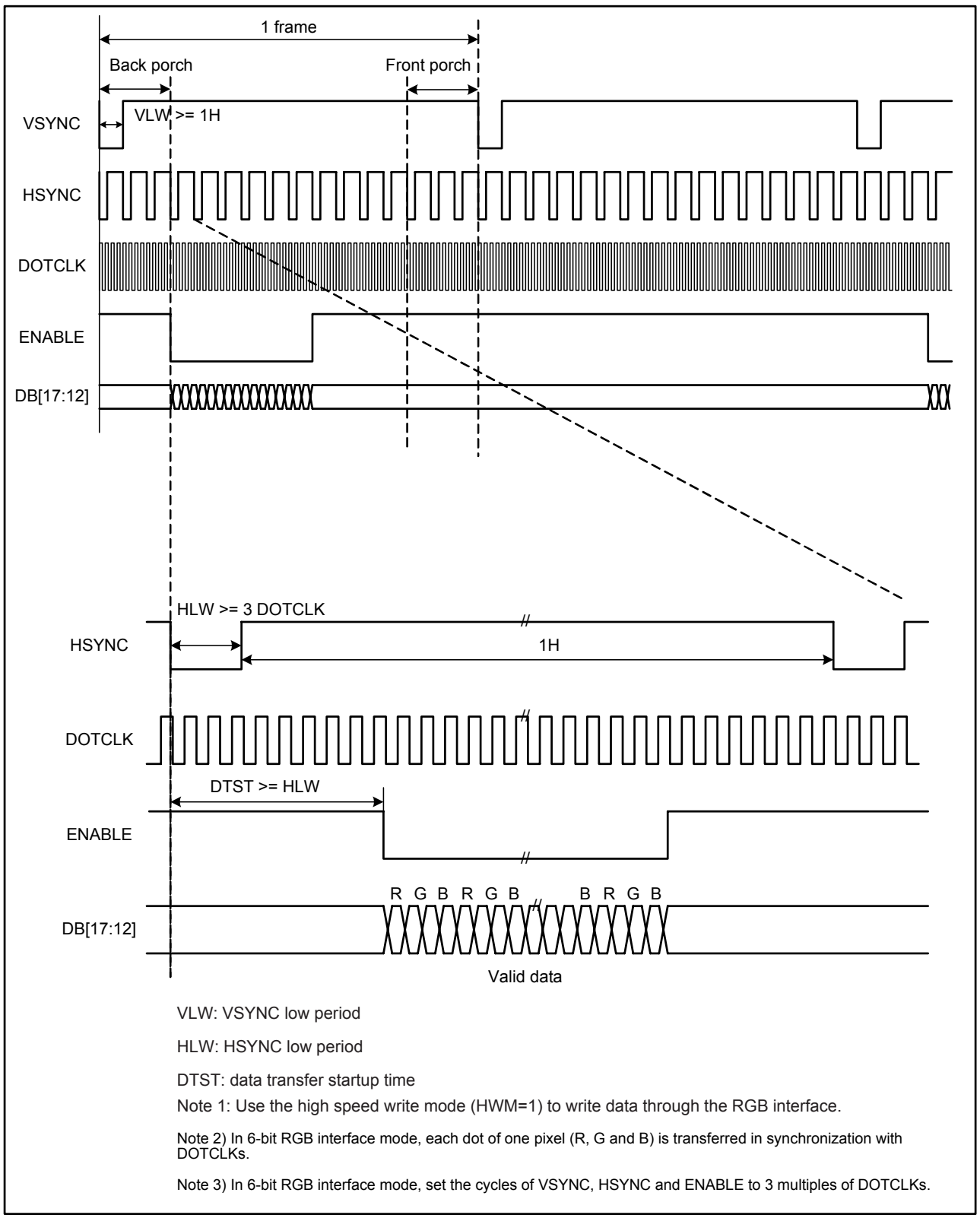


Figure16 Timing Chart of Signals in 18-/16-bit RGB Interface Mode

The timing chart of 6-bit RGB interface mode is shown as follows.



VLW: VSYNC low period

HLW: HSYNC low period

DTST: data transfer startup time

Note 1: Use the high speed write mode (HWM=1) to write data through the RGB interface.

Note 2) In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLKs.

Note 3) In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and ENABLE to 3 multiples of DOTCLKs.

Figure17 Timing chart of signals in 6-bit RGB interface mode

7.6.3. Moving Picture Mode

ILI9326 has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following merits in displaying a moving picture.

- The window address function defined the update area of GRAM.
- Only the moving picture area of GRAM is updated.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

RAM access via a system interface in RGB-I/F mode

ILI9326 allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = “0”) and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = “1” and the index register to R202h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

The following figure illustrates the operation of the ILI9326 when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

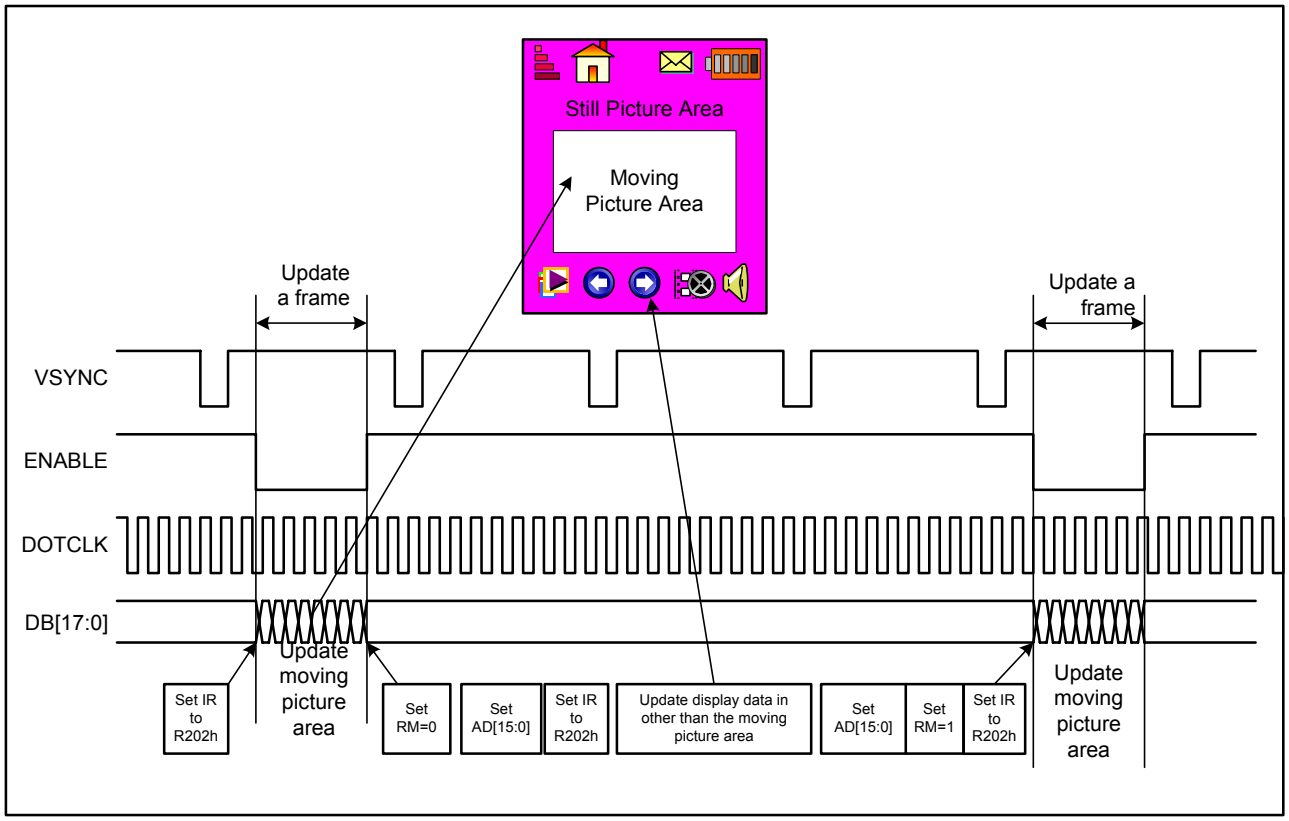


Figure18 Example of update the still and moving picture

7.6.4. 6-bit RGB Interface

The 6-bit RGB interface is selected by setting the RIM[1:0] bits to “10”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at either IOVCC1 or GND level. Registers can be set by the system interface (i80/SPI).

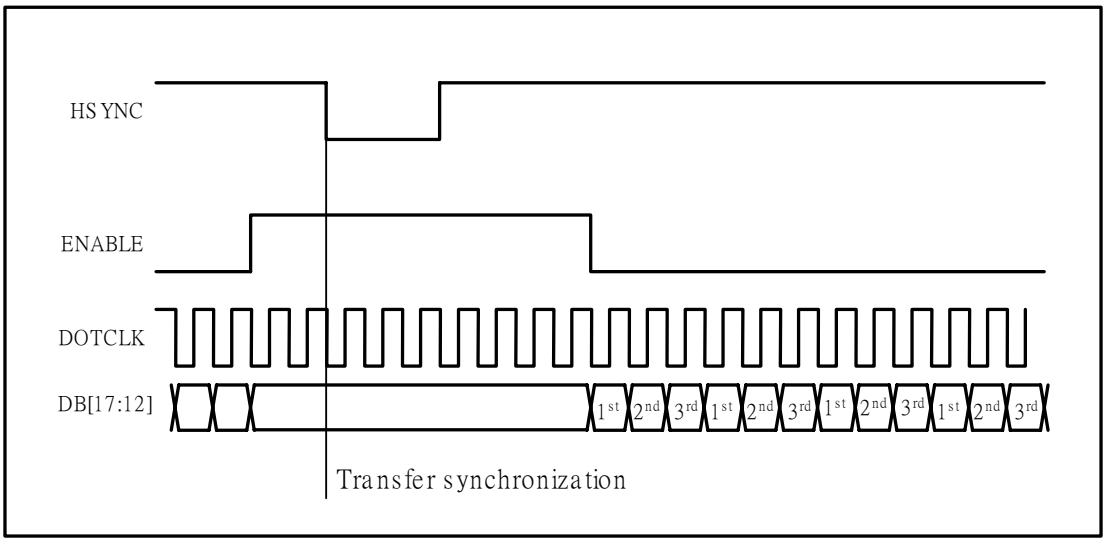
RGB interface with 6-bit data bus

	1st Transfer						2nd Transfer						3rd Transfer					
Input Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Data transfer synchronization in 6-bit RGB interface mode

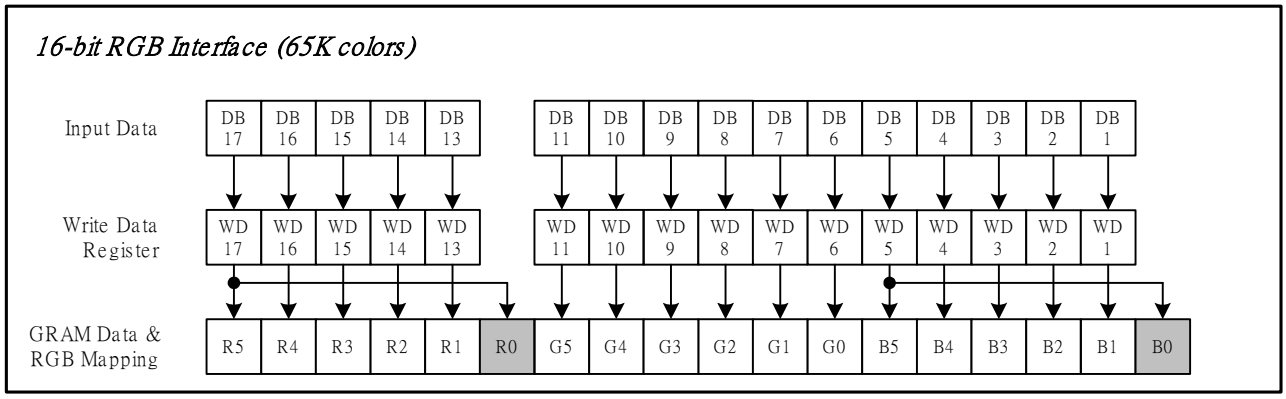
ILI9326 has data transfer counters to count the first, second, third data transfers in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.



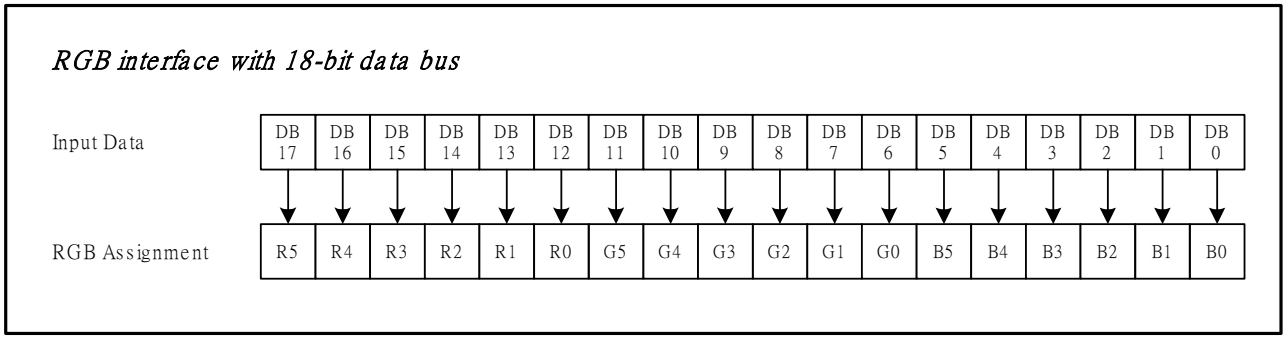
7.6.5. 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM[1:0] bits to “01”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-13, DB11-1) according to the data enable signal (ENABLE). Registers are set only via the system interface.



7.6.6. 18-bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM[1:0] bits to “00”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.



Notes in using the RGB Input Interface

1. The following are the functions not available in RGB Input Interface mode.

Function	RGB interface	I80 system interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available

2. VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.
3. The periods set with the NO[1:0] bits (gate output non-overlap period), STD[1:0] bits (source output delay period) and EQ[1:0] bits (equalization period) are not based on the internal clock but based on DOTCLK in

RGB interface mode.

4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
6. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.
7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
8. In RGB interface mode, a RAM address (AD[15:0]) is set in the address counter every frame on the falling edge of VSYNC.

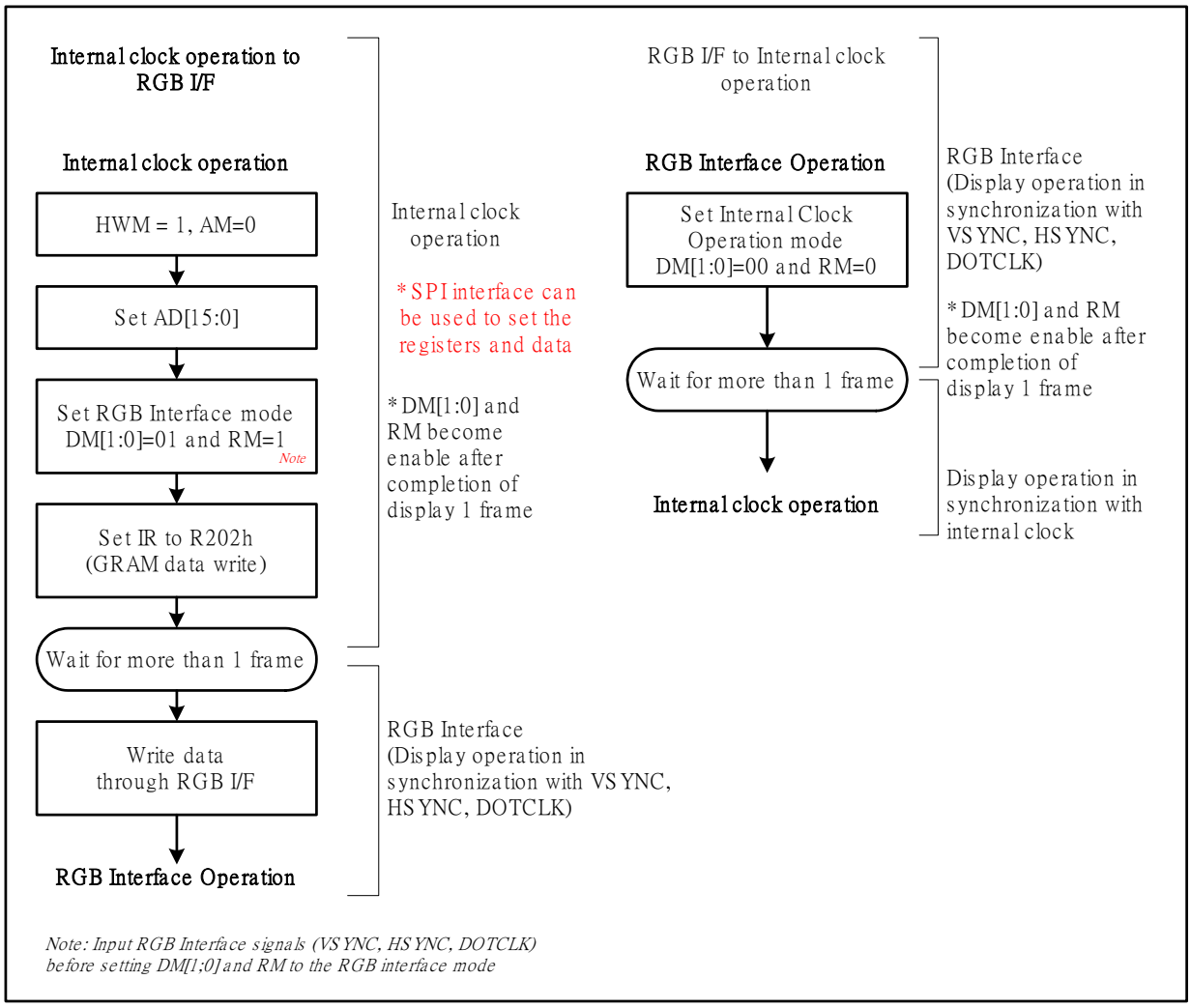


Figure19 Internal clock operation/RGB interface mode switching

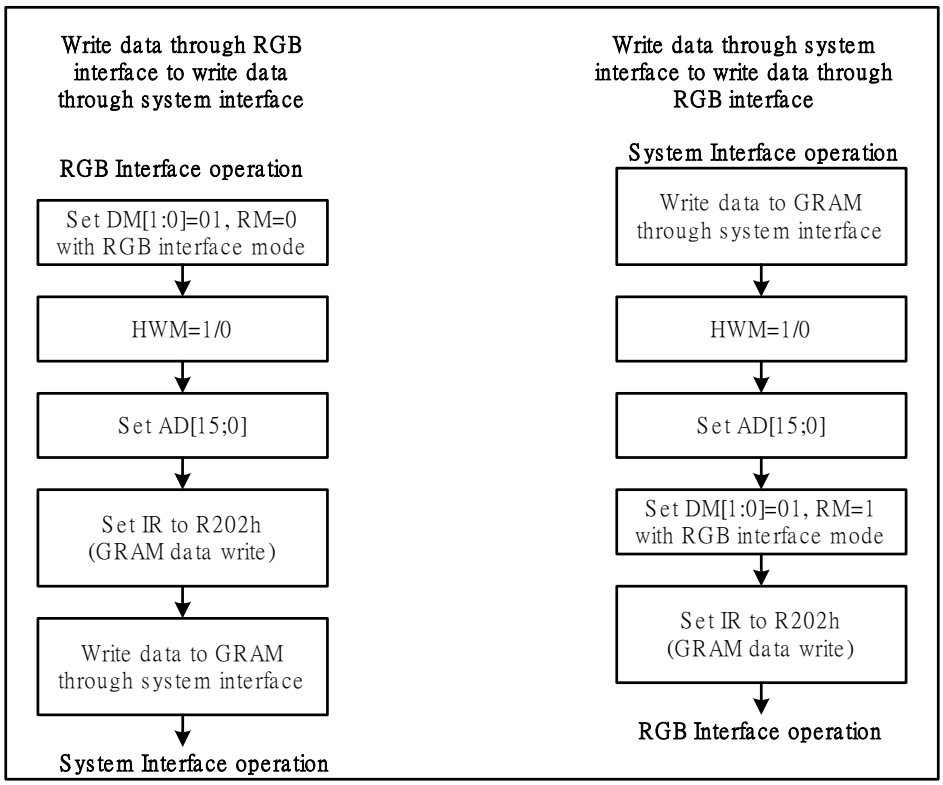


Figure20 GRAM access between system interface and RGB interface

7.7. Interface Timing

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.

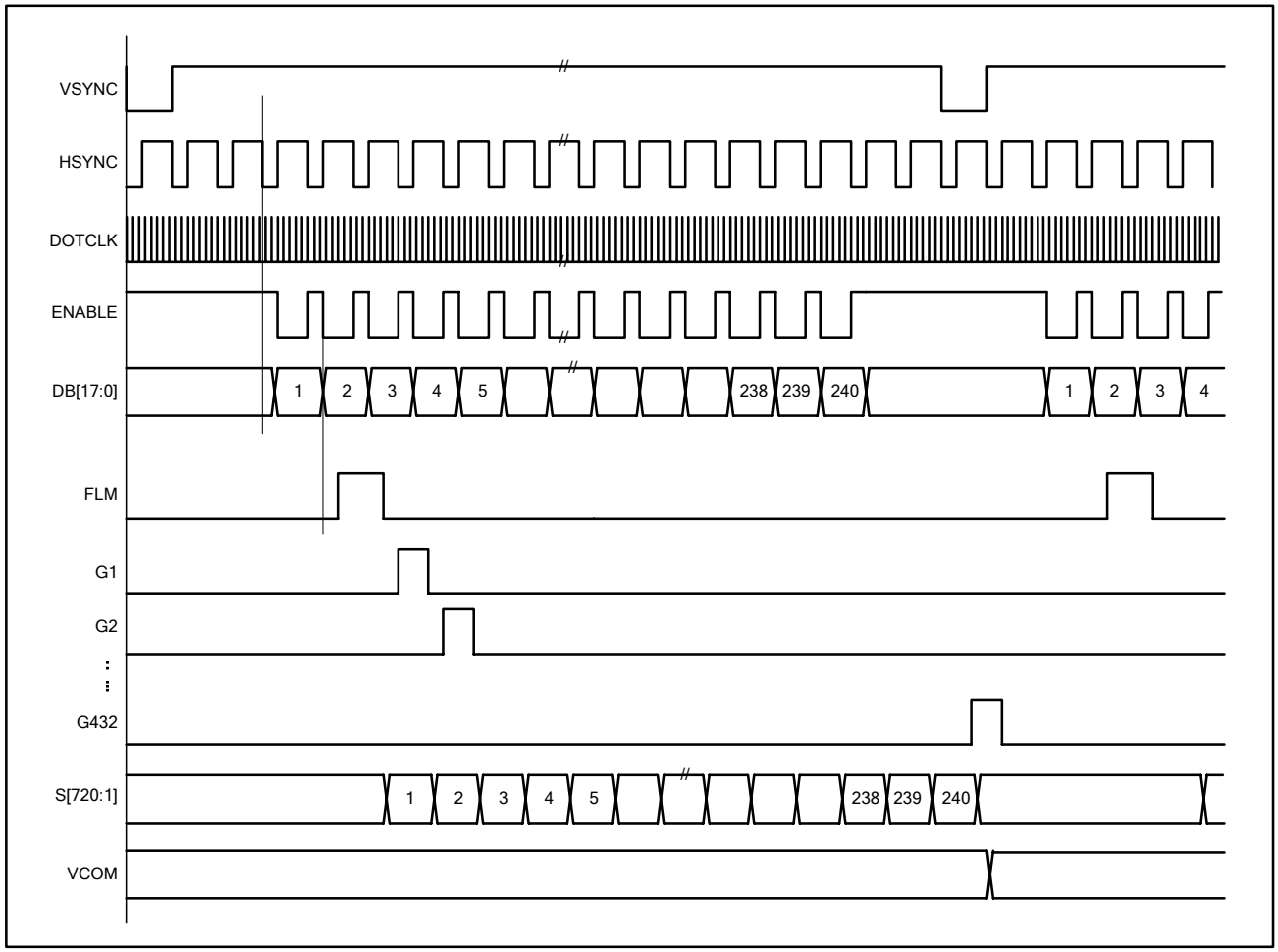


Figure21 Relationship between RGB I/F signals and LCD Driving Signals for Panel

8. Register Descriptions

8.1. Registers Access

ILI9326 adopts 18-bit bus interface architecture for high-performance microprocessor. All the functional blocks of ILI9326 starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (nRD/nWR) and data bus D17-0 are used to read/write the instructions and data of ILI9326. The registers of the ILI9326 are categorized into the following groups.

1. Specify the index of register (IR)
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address (AC)
7. Transfer data to/from the internal GRAM (R22)
8. Internal grayscale γ-correction (R30 ~ R39)

Normally, the display data (GRAM) is most often updated, and in order since the ILI9326 can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there are fewer loads on the program in the microprocessor. As the following figure shows, the way of assigning data to the 16 register bits (D[15:0]) varies for each interface. Send registers in accordance with the following data transfer format.

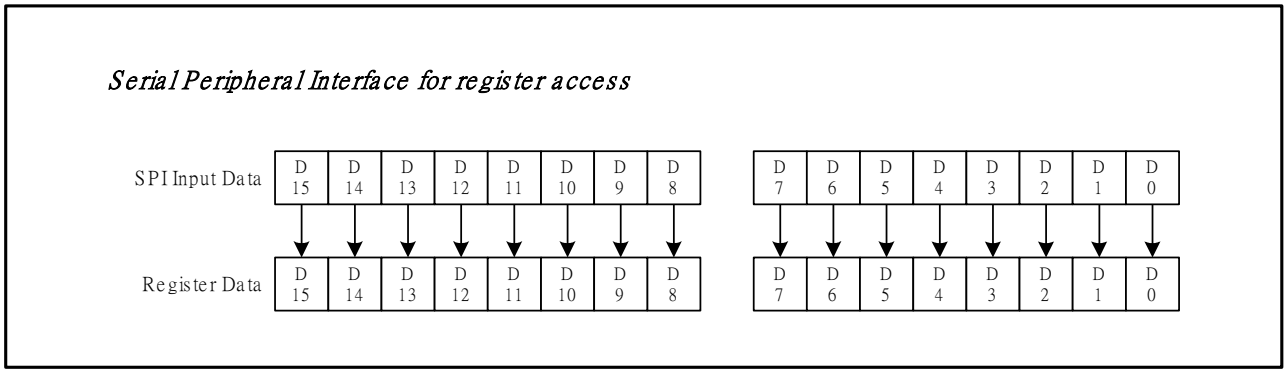


Figure22 Register Setting with Serial Peripheral Interface (SPI)

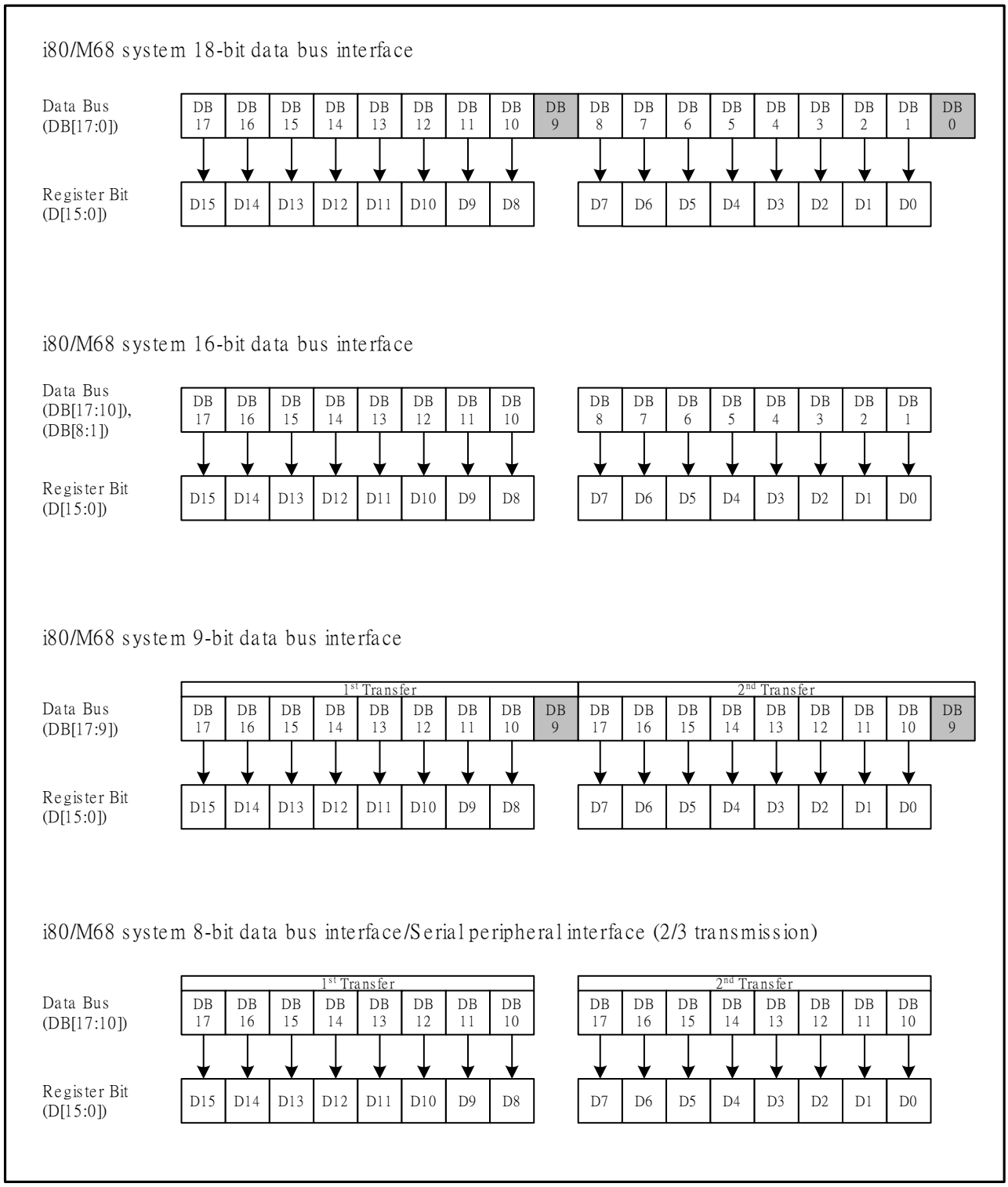


Figure23 Register setting with i80 System Interface

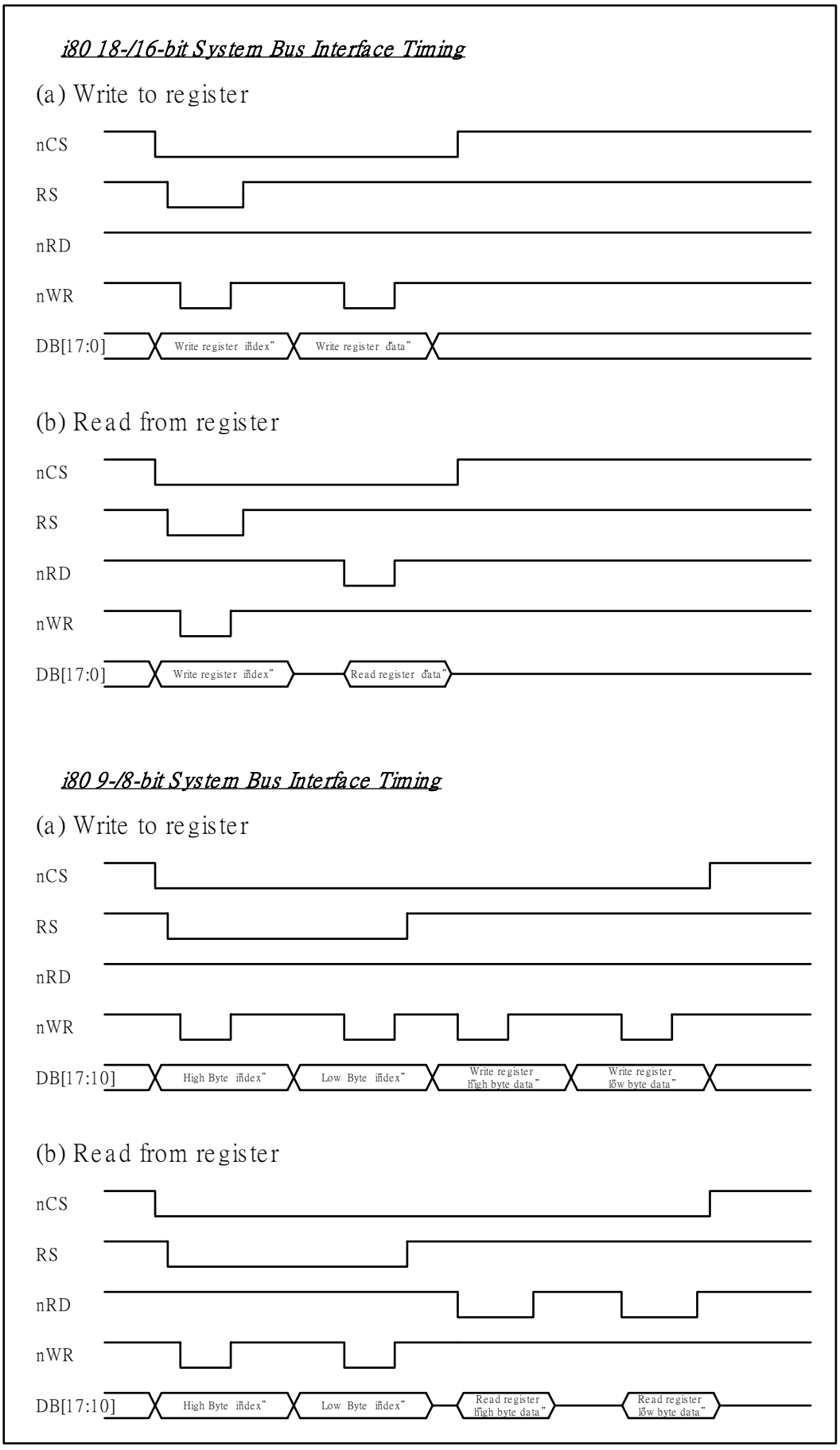


Figure 24 Register Read/Write Timing of i80 System Interface

8.2. Instruction Descriptions

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
001h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
002h	LCD Driving Control	W	1	0	0	0	0	0	0	0	B/C	0	0	NW[5]	NW[4]	NW[3]	NW[2]	NW[1]	NW[01]
003h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D1	I/D0	AM	0	EPF[1]	EPF[0]
006h	Outline Sharpening Control	W	1	EGMODE	0	0	0	0	0	AVST[2]	AVST[1]	AVST[0]	ADST[2]	ADST[1]	ADST[0]	DTHU[1]	DTHU [0]	DTHL[1]	DTHL [0]
007h	Display Control 1	W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	VON	GON	DTE	0	0	D1	D0
008h	Display Control 2	W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
009h	Display Control 3	W	1	0	0	0	0	PTV	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
00Bh	Low Power Control	W	1	0	0	0	0	0	0	0	0	0	0	0	VEM	0	0	0	COL
00Ch	RGB Display Interface Control 1	W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
00Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
010h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
011h	Panel Interface Control 2	W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	SDTI2	SDTI1	SDTI0
012h	Panel Interface Control 3	W	1	0	0	0	0	0	VEQWI1	VEQWI0	0	0	0	0	0	0	0	0	0
020h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0
021h	Panel Interface Control 5	W	1	0	0	0	0	NOWE[3]	NOWE[2]	NOWE[1]	NOWE[0]	0	0	0	0	SDTE3	SDTE2	SDTE1	SDTE0
022h	Panel Interface Control 6	W	1	0	0	0	0	0	VEQWE2	VEQWE1	VEQWE0	0	0	0	0	0	0	0	0
090h	Frame Marker Position			FMKM	FMI2	FMI1	FMI0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
100h	Power Control 1			0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
101h	Power Control 2			0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
102h	Power Control 3			0	0	0	0	0	0	0	0	VREG1R	0	0	PON	VRH3	VRH2	VRH1	VRH0
103h	Power Control 4			0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
107h	Power Control 5			0	0	0	0	0	0	0	0	0	0	DCM1	DCM0	DCT3	DCT2	DCT1	DCT0
200h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
201h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
202h	Write Data to GRAM	W	1	D[17:0] write to GRAM															
20Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS3	FRS2	FRS1	FRS0
210h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
211h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
212h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
213h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
280h	User Identification Code	R	1	0	0	0	0	0	0	0	0	0	0	0	0	UID3	UID2	UID1	UID0
281h	VCOM High Voltage (VCOMH)	W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
290h	MTP VCM Programming	W	1	UID_PGM_EN	0	0	0	VCM_PGM_EN	0	0	0	0	0	MTP_D5	MTP_D4	MTP_D3	MTP_D2	MTP_D1	MTP_D0
291h	MTP VCM Status and Enable	R/W		PGM_CNT1	PGM_CNT0	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0	0	0	0	0	0	0	0	VCM_EN
295h	MTP Programming Key	R/W		KEY15	KEY14	KEY13	KEY12	KEY11	KEY10	KEY9	KEY8	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
300h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
301h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
302h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
305h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
306h	Gamma Control 5	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]

307h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
308h	Gamma Control 7	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
309h	Gamma Control 8	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
30Ch	Gamma Control 9	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
30Dh	Gamma Control 10	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]
400h	Base Image Display Control 1	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
401h	Base Image Display Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
404h	Base Image Display Control 3	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
500h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
510h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
502h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
503h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
504h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
505h	Partial Image 2 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10

8.2.1. Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	-	-	-	-	-	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the address of register (R000h ~ R7FFh) or RAM which will be accessed.

8.2.2. Device ID Read (R000h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	1	0	0	1	0	0	1	1	0	0	1	0	0	1	1	0

The device code “9326”h is read out when read this register.

8.2.3. Driver Output Control (R001h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Select the shift direction of outputs from the source driver.

When SS = 0, the shift direction of outputs is from S1 to S720

When SS = 1, the shift direction of outputs is from S720 to S1.

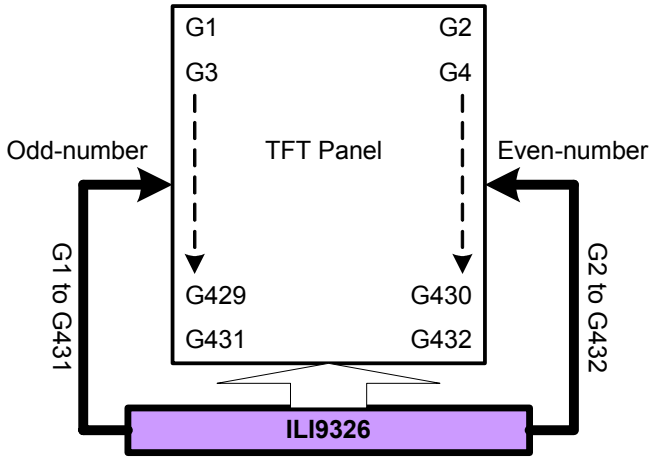
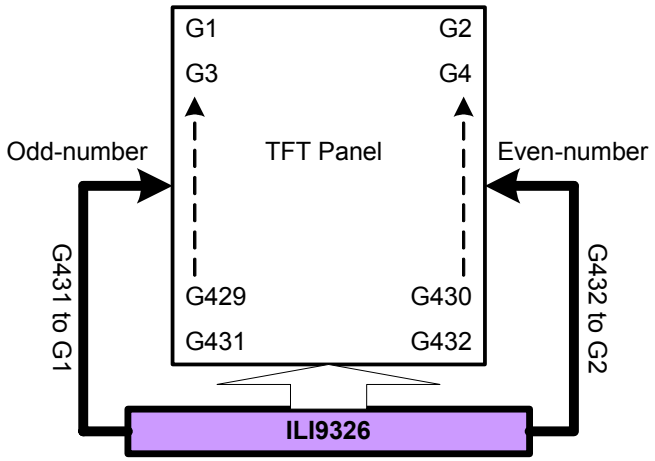
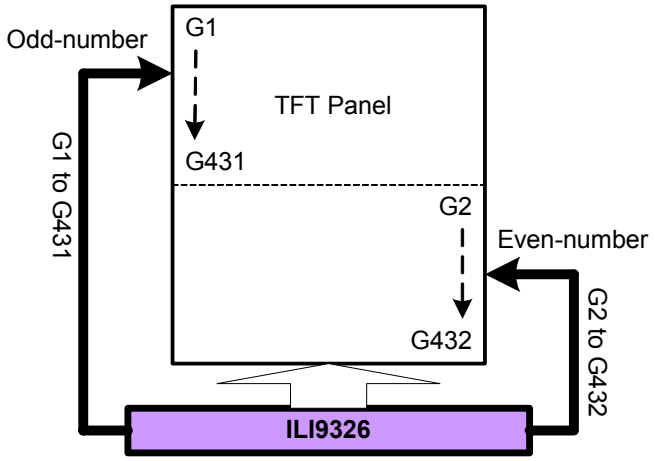
In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

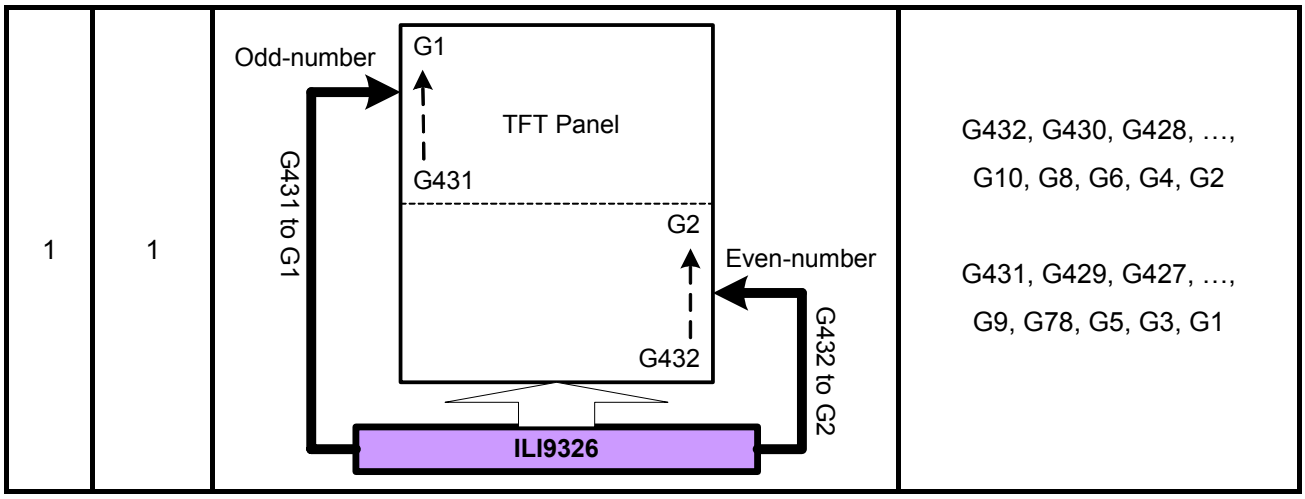
To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.

To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.

When changing SS or BGR bits, RAM data must be rewritten.

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1, G2, G3, G4, …,G428 G429, G430, G431, G432
0	1		G432, G431, G430, …, G6, G5, G4, G3, G2, G1
1	0		G1, G3, G5, G7, …,G423 G425, G427, G429, G431 G2, G4, G6, G8, …,G424 G426, G428, G430, G432



8.2.4. LCD Driving Wave Control (R002h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	B/C	0	0	NW[5]	NW[4]	NW[3]	NW[2]	NW[1]	NW[01]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

B/C Frame/line inversion selection

0 : Frame inversion

1 : Line inversion

NW[5:0] Sets "n" for the line inversion

The polarity is inverted at an interval of n+1 lines

8.2.5. Entry Mode (R003h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	TRI	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D1	I/D0	AM	0	EPF[1]	EPF[0]
Default		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

AM Control the GRAM update direction.

When AM = "0", the address is updated in horizontal writing direction.

When AM = "1", the address is updated in vertical writing direction.

When a window area is set by registers R210h ~R213h, only the addressed GRAM area is updated based on I/D[1:0] and AM bits setting.

I/D[1:0] Control the address counter (AC) to automatically increase or decrease by 1 when update one pixel display data. Refer to the following figure for the details.

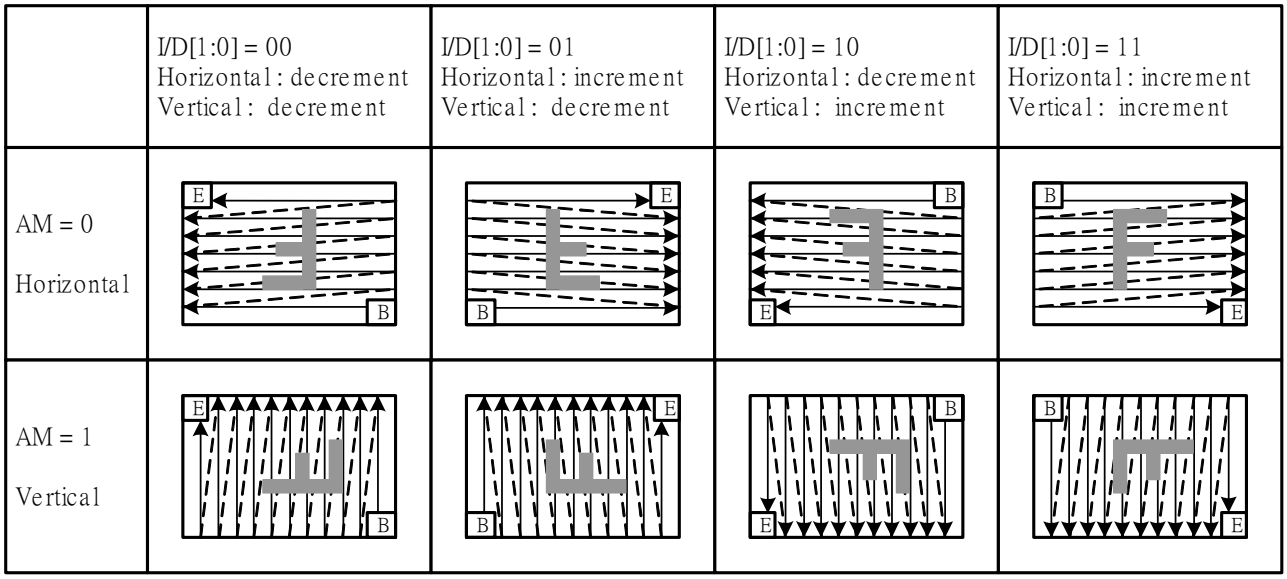


Figure25 GRAM Access Direction Setting

ORG Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data with the window address area using high-speed RAM write.

ORG = "0": The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.

ORG = "1": The original address "00000h" moves according to the I/D[1:0] setting.

Notes: 1. When ORG=1, only the origin address address"00000h" can be set in the RAM address set registers R20h, and R21h.

2. In RAM read operation, make sure to set ORG=0.

HWM High speed write function control for the GRAM data writing.

HWM="0": High speed write function disabled.

HWM="1": High speed write function enabled. When HWM=1, make sure that AM=0.

BGR Swap the R and B order of written data.

BGR="0": Follow the RGB order to write the pixel data.

BGR="1": Swap the RGB data to BGR in writing into GRAM.

TRI When TRI = "1", data are transferred to the internal RAM in 8-bit x 3 transfers mode via the 8-bit interface. It is also possible to send data via the 16-bit interface or SPI in the transfer mode that realizes display in 262k colors in combination with DFM bits. When not using these interface modes, be sure to set TRI = "0".

DFM Set the mode of transferring data to the internal RAM when TRI = "1". See the following figures for details.

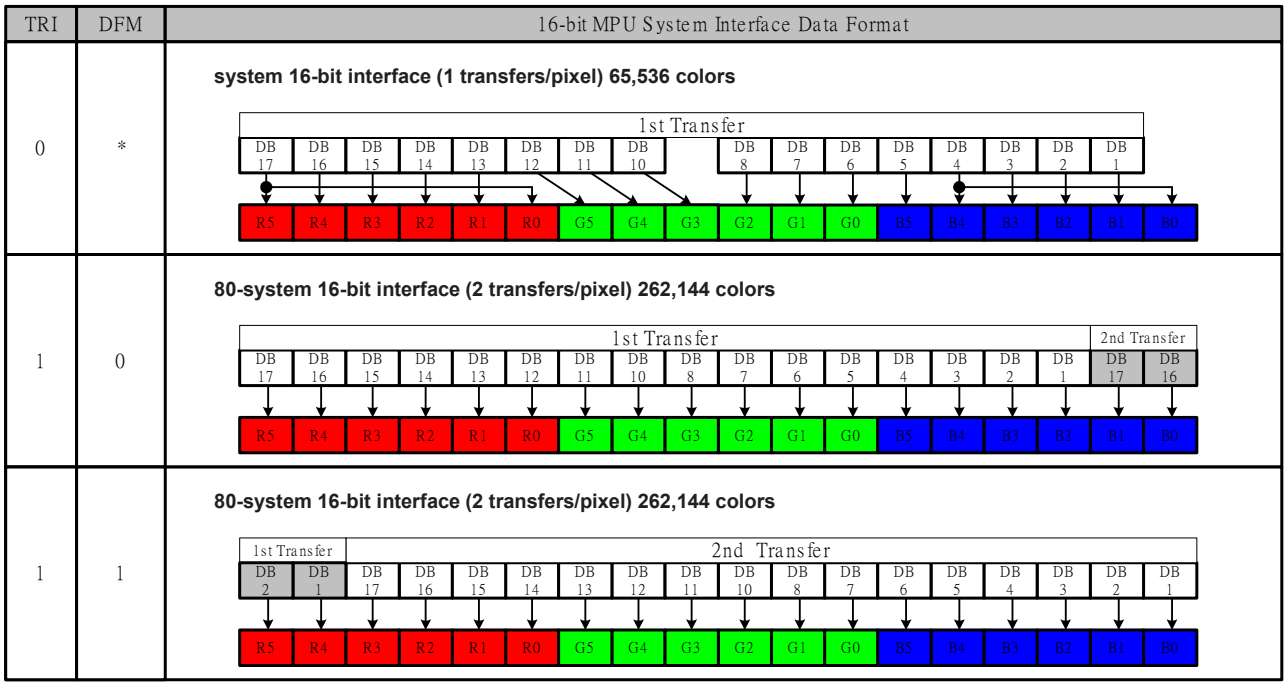


Figure26 16-bit MPU System Interface Data Format

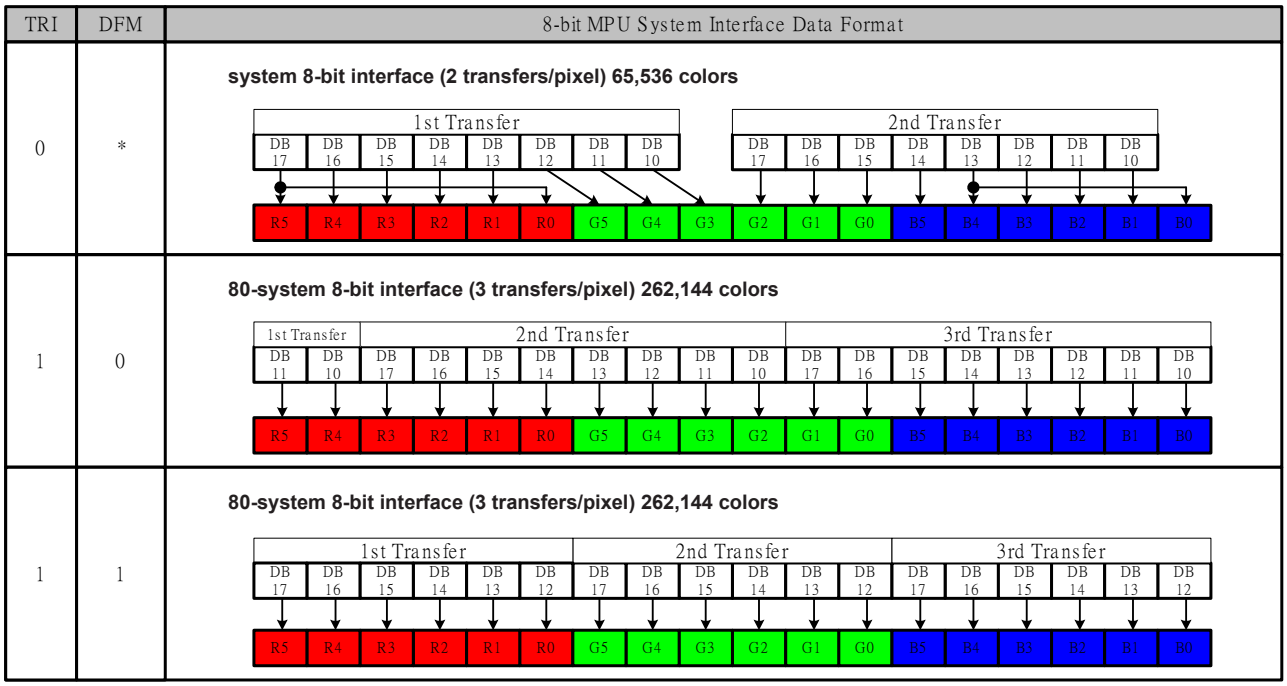


Figure27 8-bit MPU System Interface Data Format

EPF[1:0] Set the data format when 16bbp (R,G,B) to 18 bbp (r, g, b) is stored in the internal GRAM. EFP settings are only effective when:

1. i80-system 16-bit interface, TRI=0
2. i80-system 8-bit interface, TRI=0
3. MDDI, DFM=1

4.

EPF[1:0]	Expand 16bbp (R,G,B) to 18 bbp (R, G, B)
00	MSB is inputted to LSB r[5:0] = {R[4:0], R[4]} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], B[4]}
01	"0" is inputted to LSB r[5:0] = {R[4:0], 0} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], 0} Exception: R[4:0], B[4:0]=5'h1F → r[5:0], b[5:0] = 6'h3F
10	"1" is inputted to LSB r[5:0] = {R[4:0], 1} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], 1} Exception: R[4:0], B[4:0]=5'h00 → r[5:0], b[5:0] = 6'h00
11	Setting disabled

8.2.6. Outline Sharpening (R006h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	EGMODE	0	0	0	0	0	AVST2	AVST1	AVST0	ADST2	ADST1	ADST0	DTHU1	DTHU0	DTHL1	DTHL0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EGMODE: Sets outline sharpening mode when EGMODE=1.

When outline sharpening function is enabled, data is written into GRAM according to outline sharpening process.

AVST[2:0]: Sets coefficients of smoothing edges between neighboring pixels.

AVST[2:0]	Coefficients
3'h0	0.125
3'h1	0.250
3'h2	0.375
3'h3	0.500
3'h4	0.625
3'h5	0.750
3'h6	0.875
3'h7	1.000

ADST[2:0]: Sets the added coefficients for the outline sharpening operation.

ADST[2:0]	Added Coefficients
3'h0	0.0
3'h1	0.5
3'h2	1.0
3'h3	1.5

3'h4	2.0
3'h5	2.5
3'h6	3.0
3'h7	3.5

DTHU[1:0]: Sets the higher threshold of the brightness band of the object on which edge enhancement is performed.

DTHU[1:0]	Higher Threshold
2'h0	15
2'h1	31
2'h2	47
2'h3	63

DTHL[1:0]: Sets the lower threshold of the brightness band of the object on which edge enhancement is performed.

DTHL[1:0]	Lower Threshold
2'h0	0
2'h1	Setting disabled
2'h2	1
2'h3	2

8.2.7. Display Control 1 (R007h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	VON	GON	DTE	0	0	D1	D0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D[1:0] Set D[1:0]="11" to turn on the display panel, and D[1:0]="00" to turn off the display panel.

A graphics display is turned on the panel when writing D1 = "1", and is turned off when writing D1 = "0".

When writing D1 = "0", the graphics display data is retained in the internal GRAM and the ILI9326 displays the data when writing D1 = "1". When D1 = "0", i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D[1:0] = "01", the ILI9326 continues internal display operation.

When the display is turned off by setting D[1:0] = "00", the ILI9326 internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF.

D1	D0	BASEE	Source Output	FMARK Signal	ILI9326 internal operation
0	0	-	GND	Halt	Halt
0	1	-	GND	Operate	Operate
1	0	-	Non-lit display	Operate	Operate

1	1	0	Non-lit display	Operate	Operate
1	**1**	**1**	**Base image display**	**Operate**	**Operate**

Note: 1. data write operation from the microcontroller is performed irrespective of the setting of D[1:0] bits.

2. The D[1:0] setting is valid on both 1st and 2nd displays.

3. The non-lit display level from the source output pins is determined byPTS[2:0] setting.

GON and DTE Set the output level of gate driver G1 ~ G432 as follows

APE	GON	DTE	G1 ~G432 Gate Output
0	-	-	GND
1	0	0	VGH
	0	1	VGH
	1	0	VGL
	1	**1**	**VGH/VGL Normal Display**

VON Start VCOM output when VON=1. VCOM amplitude is decided by combination of VCON and VCOMG bits settings.

VON	VCOMG	VCOM output
0	0	GND
0	1	GND
1	0	Amplitude= VCOMH - GND
1	**1**	Amplitude= VCOMH - VCOML

BASEE Base image display enable bit.

When BASEE = “0”, no base image is displayed. ILI9326 drives liquid crystal at non-lit display level or displays only partial images.

When BASEE = “1”, the base image is displayed. The D[1:0] setting has higher priority over the BASEE setting.

PTDE[1:0] Partial image 2 and Partial image 1 enable bits

PTDE1/0 = 0: turns off partial image. Only base image is displayed.

PTDE1/0 = 1: turns on partial image. Set the base image display enable bit to 0 (BASEE = 0).

8.2.8. Display Control 2 (R008h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
Default		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FP[3:0]/BP[3:0]

The FP[3:0] and BP[3:0] bits specify the line number of front and back porch periods respectively.

When setting the FP[3:0] and BP[3:0] value, the following conditions shall be met:

BP + FP ≤ 16 lines

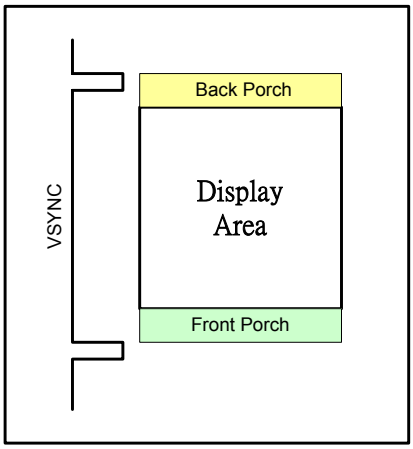
FP ≥ 2 lines

BP ≥ 2 lines

Set the BP[3:0] and FP[3:0] bits as below for each operation modes

Operation Mode	BP	FP	BP+FP
I80 System Interface Operation Mode	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
RGB interface Operation	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
VSYNC interface Operation	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP = 16 lines

FP[3:0]	Number of lines for Front Porch
BP[3:0]	**Number of lines for Back Porch**
0000	Setting Prohibited
0001	Setting Prohibited
0010	2 lines
0011	3 lines
0100	4 lines
0101	5 lines
0110	6 lines
0111	7 lines
1000	8 lines
1001	9 lines
1010	10 lines
1011	11 lines
1100	12 lines
1101	13 lines
1110	14 lines
1111	Setting Prohibited



Note: The output timing to the LCD is delayed by 2 lines period from the input of synchronizing signal.

8.2.9. Display Control 3 (R009h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	PTV	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ISC[3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG[1:0]=”10” to select interval scan. Then scan cycle is set as odd number from 0~31 frame periods. The polarity is inverted every scan cycle.

ISC3	ISC3	ISC3	ISC3	Scan Cycle	f_{FLM}=60 Hz
0	0	0	0	0 frame	-
0	0	0	1	3 frame	50ms
0	0	1	0	5 frame	84ms
0	0	1	1	7 frame	117ms
0	1	0	0	9 frame	150ms
0	1	0	1	11 frame	184ms
0	1	1	0	13 frame	217ms
0	1	1	1	15 frame	251ms
1	0	0	0	17 frame	284ms
1	0	0	1	19 frame	317ms
1	0	1	0	21 frame	351ms
1	0	1	1	23 frame	384ms
1	1	0	0	25 frame	418ms

1	1	0	1	27 frame	451ms
1	1	1	0	29 frame	484ms
1	1	1	1	31 frame	518ms

PTG[1:0] Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	Vcom output
0	**0**	**Normal scan**	**Set with the PTS[2:0] bits**	**VcomH/VcomL**
0	1	Setting Prohibited	-	-
1	0	Interval scan	Set with the PTS[2:0] bits	VcomH/VcomL
1	1	Setting Prohibited	-	-

PTS[2:0]

Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

PTS[2:0]	Source output level		Grayscale amplifier in operation	Step-up clock frequency
	Positive polarity	Negative polarity		
000	V63	V0	V63 to V0	Register Setting(DC1, DC0)
001	Setting Prohibited	Setting Prohibited	-	-
010	GND	GND	V63 to V0	Register Setting(DC1, DC0)
011	Hi-Z	Hi-Z	V63 to V0	Register Setting(DC1, DC0)
100	V63	V0	V63 and V0	1/2 frequency setting by DC1, DC0
101	Setting Prohibited	Setting Prohibited	-	-
110	GND	GND	V63 and V0	1/2 frequency setting by DC1, DC0
111	Hi-Z	Hi-Z	V63 and V0	1/2 frequency setting by DC1, DC0

Notes: 1. The power efficiency can be improved by halting grayscale amplifiers and slowing down the step-up clock frequency only in non-display drive period.

2. The gate output level in non-lit display area drive period is determined by PTG[1:0].

PTV Set the VCOM output in non-display area drive period.

PTV	VCOM operation in non-lit display drive period
0	Normal operation
1	Halts VCOM operation

8.2.10. Low Power Control (R00Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	VEM	0	0	0	COL
Default		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

COL 8-color display mode selection.

COL	Display color
0	262,144 colors

1	8 colors

VEM VCOM equalize selection.

VEM	VCOM Equalize selection
0	Disabled
1	Enable

Note: make sure that VCI <VCOMH and GND > VCOML, when using this function.

8.2.11. RGB Display Interface Control 1 (R00Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0] Select the RGB interface data width.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (1 transfer/pixel), DB[17:0]
0	1	16-bit RGB interface (1 transfer/pixel), DB[17:13] and DB[11:1]
1	0	6-bit RGB interface (3 transfers/pixel), DB[17:12]
1	1	Setting disabled

Note1: Registers are set only by the system interface.

Note2: Be sure that one pixel (3 dots) data transfer finished when interface switch.

DM[1:0] Select the display operation mode.

DM1	DM0	Display Interface
0	0	Internal system clock
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

RM Select the interface to access the GRAM.

Set RM to “1” when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM[1:0]
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM[1:0] = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
Rewrite still picture area while RGB interface		System interface	RGB interface

Displaying moving pictures.		(RM = 0)	(DM[1:0] = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Note 1: Registers are set only via the system interface or SPI interface.

Note 2: Refer to the flowcharts of "RGB Input Interface" section for the mode switch.

ENC[2:0] Set the GRAM write cycle through the RGB interface

ENC[2:0]	GRAM Write Cycle (Frame periods)
000	1 Frame
001	2 Frames
010	3 Frames
011	4 Frames
100	5 Frames
101	6 Frames
110	7 Frames
111	8 Frames

8.2.12. RGB Display Interface Control 2 (R00Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPL: Sets the signal polarity of the DOTCLK pin.

DPL = "0" The data is input on the rising edge of DOTCLK

DPL = "1" The data is input on the falling edge of DOTCLK

EPL: Sets the signal polarity of the ENABLE pin.

EPL = "0" The data DB17-0 is written when ENABLE = "0". Disable data write operation when ENABLE = "1".

EPL = "1" The data DB17-0 is written when ENABLE = "1". Disable data write operation when ENABLE = "0".

HSPL: Sets the signal polarity of the SYNC pin.

HSPL = "0" Low active

HSPL = "1" High active

VSPL: Sets the signal polarity of the VSYNC pin.

VSPL = "0" Low active

VSPL = "1" High active

8.2.13. Panel Interface Control 1 (R010h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
Default		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

RTNI[4:0]: Sets 1H (line) clock number of internal clock operating mode. In this mode, ILI9326 display operation is synchronized with internal clock signal.

RTNI[4:0]	Clocks/Line
00000~01111	Setting Disabled
10000	16 clocks
10001	17 clocks
10010	18 clocks
10011	19 clocks
10100	20 clocks
10101	21 clocks
10110	22 clocks
10111	23 clocks

RTNI[4:0]	Clocks/Line
11000	24 clocks
11001	25 clocks
11010	26 clocks
11011	27 clocks
11100	28 clocks
11101	29 clocks
11110	30 clocks
11111	31 clocks

DIVI[1:0]: Sets the division ratio of internal clock frequency.

DIVI1	DIVI0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

8.2.14. Panel Interface Control 2 (R011h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	SDTI2	SDTI1	SDTI0
Default		0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

NOWI[2:0]: Sets the gate output non-overlap period when the ILI9326 display operation is synchronized with internal clock signal.

NOWI[2:0]	Gate Non-overlap Period
000	0 clocks
001	1 clocks
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks
111	7 clocks

Note: The gate output non-overlap period is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI), from the reference point.

SDTI[2:0]: Sets the source output delay period from the reference point.

SDTI[2:0]	Source output delay period
000	0 clocks
001	1 clocks
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks

110	6 clocks
111	7 clocks

Note:

1. The number of clocks in the table setting is measured from the reference point.
2. 1 clock = internal oscillation clock period x division ratio.

8.2.15. Panel Interface Control 3 (R012h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	VEQWI1	VEQWI0	0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VEQWI[1:0]: Sets low power VCOM drive period.

VEQWI[1:0]	Source Output Position
00	0 (internal clock)
01	1 clocks
10	2 clocks
11	3 clocks

Note: The internal clock is the frequency divided clock, which is set by DIVI[1:0] bits.

8.2.16. Panel Interface Control 4 (R020h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0
Default		0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0

RTNE[5:0]: Sets RTNE in combination with DIVE so that the number of DOTCLK calculated from the following formula becomes the number of DOTCLK included in 1H (line) period, when the ILI9326 display operation is synchronized with RGB interface signals.

DIVE (division ratio) x RTNE (DOTCLKs) ≤ DOTCLKs in 1H period.

RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)
00h	Setting Prohibited	10h	16 clocks	20h	32 clocks	30h	48 clocks
01h	Setting Prohibited	11h	17 clocks	21h	33 clocks	31h	49 clocks
02h	Setting Prohibited	12h	18 clocks	22h	34 clocks	32h	50 clocks
03h	Setting Prohibited	13h	19 clocks	23h	35 clocks	33h	51 clocks
04h	Setting Prohibited	14h	20 clocks	24h	36 clocks	34h	52 clocks
05h	Setting Prohibited	15h	21 clocks	25h	37 clocks	35h	53 clocks
06h	Setting Prohibited	16h	22 clocks	26h	38 clocks	36h	54 clocks
07h	Setting Prohibited	17h	23 clocks	27h	39 clocks	37h	55 clocks
08h	Setting Prohibited	18h	24 clocks	28h	40 clocks	38h	56 clocks
09h	Setting Prohibited	19h	25 clocks	29h	41 clocks	39h	57 clocks
0ah	Setting Prohibited	1ah	26 clocks	2ah	42 clocks	3ah	58 clocks
0bh	Setting Prohibited	1bh	27 clocks	2bh	43 clocks	3bh	59 clocks
0ch	Setting Prohibited	1ch	28 clocks	2ch	44 clocks	3ch	60 clocks
0dh	Setting Prohibited	1dh	29 clocks	2dh	45 clocks	3dh	61 clocks
0eh	Setting Prohibited	1eh	30 clocks	2eh	46 clocks	3eh	62 clocks
0fh	Setting Prohibited	1fh	31 clocks	2fh	47 clocks	3fh	63 clocks

DIVE[1:0]: Sets the division ratio of DOTCLK. The ILI9326 internal operation is synchronized with the

frequency-divided DOTCLK, the frequency of which is divided by the division ratio set by DIVE[1:0]. This setting is enabled while the ILI9326 display operation is synchronized with RGB interface signals.

DIVE[1:0]	Division Ratio	18/16-bit RGB Interface	DOTCLK=5MHz	6-bit x 3 Transfers RGB Interface	DOTCLK=5MHz
00	Setting Prohibited	Setting Prohibited	-	Setting Prohibited	-
01	1/4	4 DOTCLKS	0.8 *μs*	12 DOTCLKS	0.8 *μs*
10	1/8	8 DOTCLKS	1.6 *μs*	24 DOTCLKS	1.6 *μs*
11	1/16	16 DOTCLKS	3.2 *μs*	48 DOTCLKS	3.2 *μs*

8.2.17. Panel Interface Control 5 (R021h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	NOWE[3]	NOWE[2]	NOWE[1]	NOWE[0]	0	0	0	0	SDTE3	SDTE2	SDTE1	SDTE0
Default		0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

NOWE[2:0]: Sets the gate output non-overlap period when the ILI9326 display operation is synchronized with RGB interface signals.

NOWE[3:0]	Gate Non-overlap Period	NOWE[3:0]	Gate Non-overlap Period
0000	0 clocks	1000	8 clocks
0001	1 clocks	1001	9 clocks
0010	2 clocks	1010	10 clocks
0011	3 clocks	1011	11 clocks
0100	4 clocks	1100	12 clocks
0101	5 clocks	1101	13 clocks
0110	6 clocks	1110	14 clocks
0111	7 clocks	1111	15 clocks

Note: 1 clock = (number of data transfer/pixel) x DIVE (division ratio) [DOTCLK]

SDTE[3:0]: Sets the source output delay period from the reference point, when ILI9326 is synchronized with DOTCLK.

SDTE[3:0]	Source output delay period	SDTE[3:0]	Source output delay period
4'h0	0 clocks	4'h8	8 clocks
4'h1	1 clocks	4'h9	9 clocks
4'h2	2 clocks	4'hA	10 clocks
4'h3	3 clocks	4'hB	11 clocks
4'h4	4 clocks	4'hC	12 clocks
4'h5	5 clocks	4'hD	13 clocks
4'h6	6 clocks	4'hE	14 clocks
4'h7	7 clocks	4'hF	15 clocks

Note:

1. The number of clocks in the table setting is measured from the reference point.
2. 1 clock = DOTCLK period x division ratio.

8.2.18. Panel Interface Control 6 (R022h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	VEQWE2	VEQWE1	VEQWE0	0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VEQWE[2:0]: Sets low power VCOM drive period. This setting is enabled when ILI9326 display operation is synchronized with RGB interface clock.

VEQWE [2:0]	Source Output Position
000	Setting inhibited
001	1 clocks
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks
111	7 clocks

Note: 1 clock = number of data transfer/pixel x DIVE[2:0] DOTCLK.

8.2.19. Frame Marker Position (R090h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	FMKM	FMI2	FMI1	FMI0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMP[8:0] Sets the output position of frame cycle (frame marker).

When FMP[8:0]=0, a high-active pulse FMARK is output at the start of back porch period for one display line period (1H).

Make sure the 9'h000 ≦ FMP ≦ BP+NL+FP

FMP[8:0]	FMARK Output Position
9'h000	0th line
9'h001	1st line
9'h002	2nd line
9'h003	3rd line
.	.
.	.
.	.
9'h1BD	445th line
9'h1BE	446th line
9'h1BF	447th line

FMI[2:0] Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMKM When FMKM=1, ILI9326 starts to output FMARK signal in the output interval set by FMI[2:0] bits.

FMI[2:0]	Output Interval
000	1 frame
001	2 frame
011	4 frame
101	6 frame
Others	Setting disabled

8.2.20. Power Control 1 (R100h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	**STB**
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP: When SLP = 1, ILI9326 enters the sleep mode and the display operation stops except the RC oscillator to reduce the power consumption. In the sleep mode, the GRAM data and instructions cannot be updated except the following two instructions.

a. Exit sleep mode (SLP = “0”)

b. Start oscillation

STB: When STB = 1, ILI9326 enters the standby mode and the display operation stops except the GRAM power supply to reduce the power consumption. In the sleep mode, the GRAM data and instructions cannot be updated except the following two instructions.

a. Exit standby mode (STB = “0”)

b. Start oscillation

AP[2:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0] = “000” to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

AP[2:0]	Gamma driver amplifiers	Source driver amplifiers
000	Halt	Halt
001	1.00	1.00
010	1.00	0.75
011	1.00	0.50
100	0.75	1.00
101	0.75	0.75
110	0.75	0.50
111	0.50	0.50

SAP: Source Driver output control

SAP=0, Source driver is disabled.

SAP=1, Source driver is enabled.

When starting the charge-pump of LCD in the Power ON stage, make sure that SAP=0, and set the SAP=1, after starting up the LCD power supply circuit.

APE: Power supply enable bit.

Set APE = “1” to start the generation of power supply according to the power supply startup sequence.

BT[2:0]: Sets the factor used in the step-up circuits.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0	Vci1 x 2	- Vci1	Vci1 x 6	- Vci1 x 5
3'h1	Vci1 x 2	- Vci1		- Vci1 x 4
3'h2				- Vci1 x 3
3'h3	Vci1 x 2	- Vci1	Vci1 x 5	- Vci1 x 5
3'h4				- Vci1 x 4
3'h5				- Vci1 x 3
3'h6	Vci1 x 2	- Vci1	Vci1 x 4	- Vci1 x 4
3'h7				- Vci1 x 3

Notes: 1. Connect capacitors to the capacitor connection pins when generating DDVDH, VGH, VGL and VCL levels.

2. Make sure DDVDH = 6.0V (max.), VGH = 15.0V (max.), VGL = – 12.5V (max) and VCL= -3.0V (max.)

8.2.21. Power Control 2 (R101h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
Default		0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0

VC[2:0] Sets the ratio factor of VciLVL to generate the reference voltages VciOUT and Vci1.

VC2	VC1	VC0	VciOUT reference voltage Vci1 voltage
0	0	0	0.95 x Vci
0	0	1	0.90 x Vci
0	1	0	0.85 x Vci
0	1	1	0.80 x Vci
1	0	0	0.75 x Vci
1	0	1	0.70 x Vci
1	1	0	Disabled
1	1	1	1.0 x Vci

DC0[2:0]: Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC1[2:0]: Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC02	DC01	DC00	Step-up circuit1 step-up frequency (f_{DCDC1})
0	0	0	Fosc
0	0	1	Fosc / 2
0	1	0	Fosc / 4
0	1	1	Fosc / 8

DC12	DC11	DC10	Step-up circuit2 step-up frequency (f_{DCDC2})
0	0	0	Fosc / 4
0	0	1	Fosc / 8
0	1	0	Fosc / 16
0	1	1	Fosc / 32

1	0	0	Fosc / 16	1	0	0	Fosc / 64
1	0	1	Fosc / 32	1	0	1	Fosc / 128
1	1	0	Fosc / 64	1	1	0	Fosc / 256
1	1	1	Halt step-up circuit 1	1	1	1	Halt step-up circuit 2

Note: Be sure $f_{DCDC1} \geq f_{DCDC2}$ when setting DC0[2:0] and DC1[2:0].

8.2.22. Power Control 3 (R102h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	VREG1R	0	0	PON	VRH3	VRH2	VRH1	VRH0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VRH[3:0] Set the amplifying rate (1.6 ~ 2.4) of VciLVL applied to output the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

VREG1R: Select the external reference voltage VCILVL or internal reference voltage VCIR.

VREG1R	VREG1OUT Generating Reference Voltage
0	External reference voltage VCILVL (**default**)
1	Internal reference voltage 2.5V

VREG1R =0					VREG1R =1				
VRH3	VRH2	VRH1	VRH0	VREG1OUT	VRH3	VRH2	VRH1	VRH0	VREG1OUT
0	0	0	0	Halt	0	0	0	0	Halt
0	0	0	1	**VciLVL x 2.00**	0	0	0	1	**2.5V x 2.00 = 5.000V**
0	0	1	0	**VciLVL x 2.05**	0	0	1	0	**2.5V x 2.05 = 5.125V**
0	0	1	1	**VciLVL x 2.10**	0	0	1	1	**2.5V x 2.10 = 5.250V**
0	1	0	0	**VciLVL x 2.20**	0	1	0	0	**2.5V x 2.20 = 5.500V**
0	1	0	1	**VciLVL x 2.30**	0	1	0	1	**2.5V x 2.30 = 5.750V**
0	1	1	0	**VciLVL x 2.40**	0	1	1	0	**2.5V x 2.40 = 6.000V**
0	1	1	1	**VciLVL x 2.40**	0	1	1	1	**2.5V x 2.40 = 6.000V**
1	0	0	0	VciLVL x 1.60	1	0	0	0	2.5V x 1.60 = 4.000V
1	0	0	1	VciLVL x 1.65	1	0	0	1	2.5V x 1.65 = 4.125V
1	0	1	0	VciLVL x 1.70	1	0	1	0	2.5V x 1.70 = 4.250V
1	0	1	1	VciLVL x 1.75	1	0	1	1	2.5V x 1.75 = 4.375V
1	1	0	0	VciLVL x 1.80	1	1	0	0	2.5V x 1.80 = 4.500V
1	1	0	1	VciLVL x 1.85	1	1	0	1	2.5V x 1.85 = 4.625V
1	1	1	0	VciLVL x 1.90	1	1	1	0	2.5V x 1.90 = 4.750V
1	1	1	1	VciLVL x 1.95	1	1	1	1	2.5V x 1.95 = 4.875V

When VCI<2.5V, Internal reference voltage will be same as VCI.

Make sure that VC and VRH setting restriction: VREG1OUT ≦ (DDVDH - 0.5)V.

PON Control ON/OFF of circuit3 (VGL) output.

PON	VLOUT3 Power On/Off Control
0	VGL output is disable
1	VGL output is enable

8.2.23. Power Control 4 (R103h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0

Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VDV[4:0] Select the factor of VREG1OUT to set the amplitude of Vcom alternating voltage from 0.70 to 1.32x VREG1OUT .

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
0	0	0	0	0	VREG1OUT x 0.70
0	0	0	0	1	VREG1OUT x 0.72
0	0	0	1	0	VREG1OUT x 0.74
0	0	0	1	1	VREG1OUT x 0.76
0	0	1	0	0	VREG1OUT x 0.78
0	0	1	0	1	VREG1OUT x 0.80
0	0	1	1	0	VREG1OUT x 0.82
0	0	1	1	1	VREG1OUT x 0.84
0	1	0	0	0	VREG1OUT x 0.86
0	1	0	0	1	VREG1OUT x 0.88
0	1	0	1	0	VREG1OUT x 0.90
0	1	0	1	1	VREG1OUT x 0.92
0	1	1	0	0	VREG1OUT x 0.94
0	1	1	0	1	VREG1OUT x 0.96
0	1	1	1	0	VREG1OUT x 0.98
0	1	1	1	1	VREG1OUT x 1.00

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
1	0	0	0	0	VREG1OUT x 1.02
1	0	0	0	1	VREG1OUT x 1.04
1	0	0	1	0	VREG1OUT x 1.06
1	0	0	1	1	VREG1OUT x 1.08
1	0	1	0	0	VREG1OUT x 1.10
1	0	1	0	1	VREG1OUT x 1.12
1	0	1	1	0	VREG1OUT x 1.14
1	0	1	1	1	VREG1OUT x 1.16
1	1	0	0	0	VREG1OUT x 1.18
1	1	0	0	1	VREG1OUT x 1.20
1	1	0	1	0	VREG1OUT x 1.22
1	1	0	1	1	VREG1OUT x 1.24
1	1	1	0	0	VREG1OUT x 1.26
1	1	1	0	1	VREG1OUT x 1.28
1	1	1	1	0	VREG1OUT x 1.30
1	1	1	1	1	VREG1OUT x 1.32

Set VDV[4:0] to let Vcom amplitude less than 6V.

VCOMG Select VCOML output voltage.

VCOMG	VCOM output low voltage selection
0	VCOM output low is fixed to GND. VCOML and VCL outputs are halted.
1	VCOM output low is fixed to VCOML.

8.2.24. Power Control 5 (R107h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	DCM1	DCM0	DCT3	DCT2	DCT1	DCT0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DCT[3:]: Sets the synchronizing timing of the step-up reference clock for display operation in 1H line period.

DCM[1:0]	Step-up circuit Display synchronous function	Reference clock for step-up operation	Step-up reference clock
2'h0	Invalid	OSC clock	-
2'h1	Step-up circuit 1: Horizontal synchronous Step-up circuit 2: Vertical synchronous	Display operation clock (including DOTCLK)	RTNI setting / 1H (RTNE setting / 1H)
2'h2	Invalid	Display operation clock (including DOTCLK)	16 clocks / 1H
2'h3	Step-up circuit 1: Horizontal synchronous Step-up circuit 2: Vertical synchronous	Display operation clock (including DOTCLK)	16 clocks / 1H

8.2.25. GRAM Horizontal (R200h) / Vertical Address Set (R201h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD[16:0] Set the initial value of address counter (AC).

The address counter (AC) is automatically updated in accordance to the setting of the AM, I/D bits as data is written to the internal GRAM. The address counter is not automatically updated when read data from the internal GRAM.

AD[16:0]	GRAM Data Map
17'h00000 ~ 17'h000EF	1st line GRAM Data
17'h00100 ~ 17'h001EF	2nd line GRAM Data
17'h00200 ~ 17'h002EF	3rd line GRAM Data
17'h00300 ~ 17'h003EF	4th line GRAM Data
17'h00400 ~ 17'h004EF	5th line GRAM Data
17'h1AC00 ~ 17'h1ACEF	429th line GRAM Data
17'h1AD00 ~ 17'h1ADEF	430th line GRAM Data
17'h1AE00 ~ 17'h1AEEF	431th line GRAM Data
17'h1AF00 ~ 17'h1AFEF	432th line GRAM Data

Note1: When the RGB interface is selected (RM = "1"), the address AD[16:0] is set to the address counter every frame on the falling edge of VSYNC.

Note2: When the internal clock operation or the VSYNC interface mode is selected (RM = "0"), the address AD[16:0] is set to address counter when update register R21.

8.2.26. Write Data to GRAM (R202h)

R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM write data (WD[17:0], the DB[17:0] pin assignment differs for each interface.																	

This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

8.2.27. Read Data from GRAM (R202h)

R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	RAM Read Data (RD[17:0], the DB[17:0] pin assignment differs for each interface.																	

RD[17:0] Read 18-bit data from GRAM through the read data register (RDR).

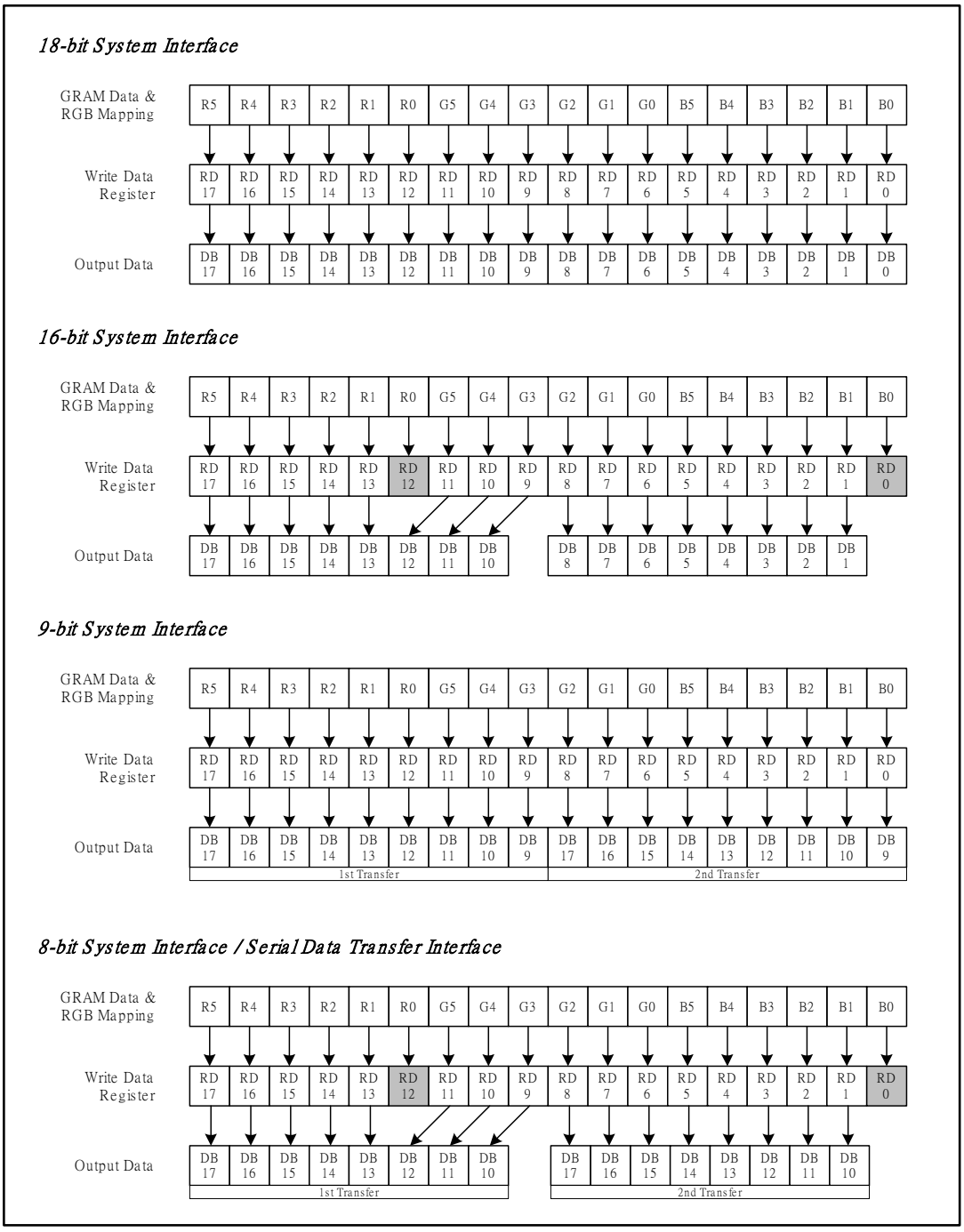


Figure 28 Data Read from GRAM through Read Data Register in 18-/16-/9-/8-bit Interface Mode

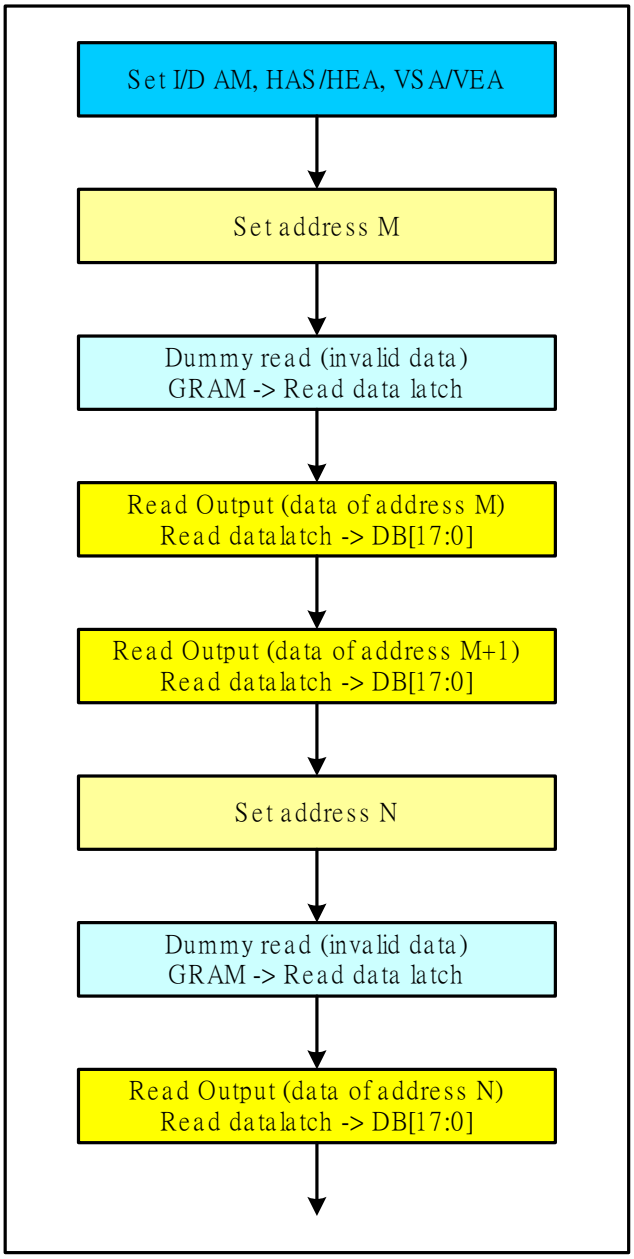


Figure 29 GRAM Data Read Back Flow Chart

8.2.28. Frame Rate and Color Control (R20Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS3	FRS2	FRS1	FRS0
Default		0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

FRS[4:0] Set the frame rate when the internal resistor is used for oscillator circuit.

FRS[3:0]	Frame Rate
0000	95
0001	80 (**default**)
0010	70
0011	60
0100	52

0101	47
0110	43
0111	40
1000	36
1001	33
1010	30

8.2.29. Horizontal and Vertical RAM Address Position (R210h, R211h, R212h, R213h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R210h	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R211h	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
	Default		0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R212h	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R213h	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
	Default		0	0	0	0	0	0	0	1	1	0	1	0	1	1	1	1

HSA[7:0]/HEA[7:0] HSA[7:0] and HEA[7:0] represent the respective addresses at the start and end of the window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA and HEA bits must be set before starting RAM write operation. In setting these bits, be sure “00”h ≤ HSA[7:0]< HEA[7:0] ≤ “EF”h. and “04”h≦HEA-HSA.

VSA[8:0]/VEA[8:0] VSA[8:0] and VEA[8:0] represent the respective addresses at the start and end of the window address area in vertical direction. By setting VSA and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting, be sure “000”h ≤ VSA[8:0]< VEA[8:0] ≤ “1AF”h.

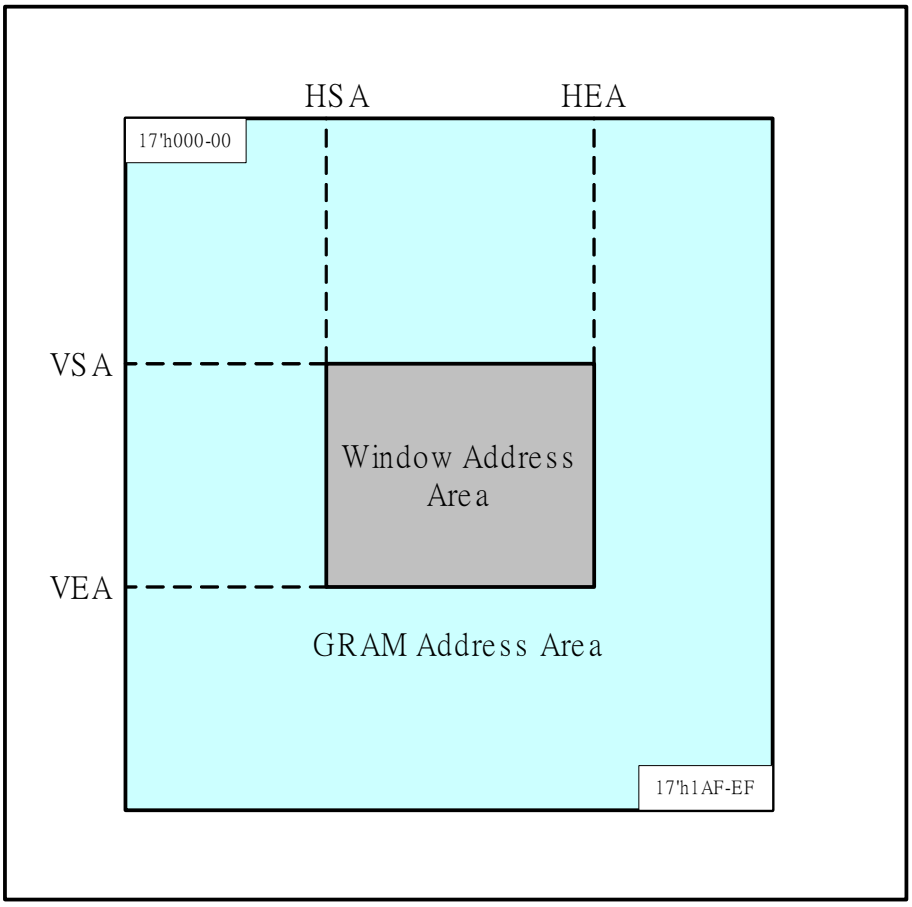


Figure 30 GRAM Access Range Configuration

"00"h ≤HAS[7:0] ≤HEA[7:0] ≤"EF"h

"00"h ≤VSA[8:0] ≤VEA[8:0] ≤"1AF"h

Note1. The window address range must be within the GRAM address space.

Note2. Data are written to GRAM in four-words when operating in high speed mode, the dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

8.2.30. User Identification Code (R280h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	0	0	0	0	0	0	0	0	0	0	UID3	UID2	UID1	UID0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

UID[3:0] : This register record the User's ID code and it's read only.

This User's ID code is recorded in the MTP, please refer to the MTP programming flow.

8.2.31. Vcom High Voltage 1 (R281h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCM[5:0] Set the internal VcomH voltage.

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH	
0	0	0	0	0	0	VREG1OUT	x 0.685
0	0	0	0	0	1	VREG1OUT	x 0.690
0	0	0	0	1	0	VREG1OUT	x 0.695
0	0	0	0	1	1	VREG1OUT	x 0.700
0	0	0	1	0	0	VREG1OUT	x 0.705
0	0	0	1	0	1	VREG1OUT	x 0.710
0	0	0	1	1	0	VREG1OUT	x 0.715
0	0	0	1	1	1	VREG1OUT	x 0.720
0	0	1	0	0	0	VREG1OUT	x 0.725
0	0	1	0	0	1	VREG1OUT	x 0.730
0	0	1	0	1	0	VREG1OUT	x 0.735
0	0	1	0	1	1	VREG1OUT	x 0.740
0	0	1	1	0	0	VREG1OUT	x 0.745
0	0	1	1	0	1	VREG1OUT	x 0.750
0	0	1	1	1	0	VREG1OUT	x 0.755
0	0	1	1	1	1	VREG1OUT	x 0.760
0	1	0	0	0	0	VREG1OUT	x 0.765
0	1	0	0	0	1	VREG1OUT	x 0.770
0	1	0	0	1	0	VREG1OUT	x 0.775
0	1	0	0	1	1	VREG1OUT	x 0.780
0	1	0	1	0	0	VREG1OUT	x 0.785
0	1	0	1	0	1	VREG1OUT	x 0.790
0	1	0	1	1	0	VREG1OUT	x 0.795
0	1	0	1	1	1	VREG1OUT	x 0.800
0	1	1	0	0	0	VREG1OUT	x 0.805
0	1	1	0	0	1	VREG1OUT	x 0.810
0	1	1	0	1	0	VREG1OUT	x 0.815
0	1	1	0	1	1	VREG1OUT	x 0.820
0	1	1	1	0	0	VREG1OUT	x 0.825
0	1	1	1	0	1	VREG1OUT	x 0.830
0	1	1	1	1	0	VREG1OUT	x 0.835
0	1	1	1	1	1	VREG1OUT	x 0.840

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH	
1	0	0	0	0	0	VREG1OUT	x 0.845
1	0	0	0	0	1	VREG1OUT	x 0.850
1	0	0	0	1	0	VREG1OUT	x 0.855
1	0	0	0	1	1	VREG1OUT	x 0.860
1	0	0	1	0	0	VREG1OUT	x 0.865
1	0	0	1	0	1	VREG1OUT	x 0.870
1	0	0	1	1	0	VREG1OUT	x 0.875
1	0	0	1	1	1	VREG1OUT	x 0.880
1	0	1	0	0	0	VREG1OUT	x 0.885
1	0	1	0	0	1	VREG1OUT	x 0.890
1	0	1	0	1	0	VREG1OUT	x 0.895
1	0	1	0	1	1	VREG1OUT	x 0.900
1	0	1	1	0	0	VREG1OUT	x 0.905
1	0	1	1	0	1	VREG1OUT	x 0.910
1	0	1	1	1	0	VREG1OUT	x 0.915
1	0	1	1	1	1	VREG1OUT	x 0.920
1	1	0	0	0	0	VREG1OUT	x 0.925
1	1	0	0	0	1	VREG1OUT	x 0.930
1	1	0	0	1	0	VREG1OUT	x 0.935
1	1	0	0	1	1	VREG1OUT	x 0.940
1	1	0	1	0	0	VREG1OUT	x 0.945
1	1	0	1	0	1	VREG1OUT	x 0.950
1	1	0	1	1	0	VREG1OUT	x 0.955
1	1	0	1	1	1	VREG1OUT	x 0.960
1	1	1	0	0	0	VREG1OUT	x 0.965
1	1	1	0	0	1	VREG1OUT	x 0.970
1	1	1	0	1	0	VREG1OUT	x 0.975
1	1	1	0	1	1	VREG1OUT	x 0.980
1	1	1	1	0	0	VREG1OUT	x 0.985
1	1	1	1	0	1	VREG1OUT	x 0.990
1	1	1	1	1	0	VREG1OUT	x 0.995
1	1	1	1	1	1	VREG1OUT	x 1.000

8.2.32. MTP VCM Programming Control (R290h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	UID_ PGM_EN	0	0	0	VCM_ PGM_EN	0	0	0	0	0	MTP_ D5	MTP_ D4	MTP_ D3	MTP_ D2	MTP_ D1	MTP_ D0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCM_PGM_EN: VCM_D[5:0] MTP programming enable. When, Set VCM_PGM_EN=1 to write VCM data into the MTP and these MTP can be programmed max. 3 times.

UID_PGM_EN: User ID UID[3:0] (R280h) programming enable.

Control bit	Description
UID_PGM_EN=0, VCM_PGM_EN=0	MTP programming disable
UID_PGM_EN=0, VCM_PGM_EN=1	VCOMH MTP (VCM[5:0]) programming enable
UID_PGM_EN=1, VCM_PGM_EN=0	User's ID (UID[3:0]) programming enable
UID_PGM_EN=1, VCM_PGM_EN=1	Setting Prohibited

MTP_D[5:0]: MTP programming data.

8.2.33. MTP VCM Status and Enable (R291h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	PGM_CNT1	PGM_CNT0	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0	0	0	0	0	0	0	0	VCM_EN
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PGM_CNT[1:0]: MTP programmed record. These bits are read only.

PGM_CNT[1:0]	Description
00	MTP clean
01	MTP programmed 1 time
10	MTP programmed 2 times
11	MTP programmed 3 times

VCM_D[5:0]: MTP VCM data read value. These bits are read only.

VCM_EN: MTP VCM data enable.

'1': Set this bit to enable MTP VCM data to replace R281h VCM value.

'0': Default value, use R281h VCM value.

8.2.34. MTP Programming ID Key (R295h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

KEY[15:0]: MTP Programming ID key protection. Before writing MTP programming data R290h, it must write R295h with 0xAA55 value first to make MTP programming successfully. If R295h is not written with 0xAA55, MTP programming will be fail. See MTP Programming flow.

8.2.35. Gamma Control (R300h ~ R30Dh)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R300h	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
R301h	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
R302h	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
R305h	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
R306h	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R307h	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
R308h	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
R309h	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
R30Ch	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
R30Dh	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

KP5-0[2:0] : γfine adjustment register for positive polarity

RP1-0[2:0] : γgradient adjustment register for positive polarity

VRP1-0[4:0] : γamplitude adjustment register for positive polarity

KN5-0[2:0] : γfine adjustment register for negative polarity

RN1-0[2:0] : γgradient adjustment register for negative polarity

VRN1-0[4:0] : γamplitude adjustment register for negative polarity

8.2.36. Base Image Display Control (R400h, R401h, R404h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R400h	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R401h	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R404h	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN[5:0] The ILI9326 allows to specify the gate line from which the gate driver starts to scan by setting the SCN[5:0] bits.

SCN[5:0]	Gate Scanning Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h	G1	G432	G1	G432
01h	G9	G424	G17	G416
02h	G17	G416	G33	G400
03h	G25	G408	G49	G384
04h	G33	G400	G65	G368
05h	G41	G392	G81	G352
06h	G49	G384	G97	G336
07h	G57	G376	G113	G320
08h	G65	G368	G129	G304
09h	G73	G360	G145	G288
0Ah	G81	G352	G161	G272
0Bh	G89	G344	G177	G256
0Ch	G97	G336	G193	G240
0Dh	G105	G328	G209	G224
0Eh	G113	G320	G225	G208
0Fh	G121	G312	G241	G192
10h	G129	G304	G257	G176
11h	G137	G296	G273	G160
12h	G145	G288	G289	G144
13h	G153	G280	G305	G128
14h	G161	G272	G321	G112
15h	G169	G264	G337	G96
16h	G177	G256	G353	G80
17h	G185	G248	G369	G64
18h	G193	G240	G385	G48
19h	G201	G232	G401	G32
1Ah	G209	G224	G417	G16
1Bh	G217	G216	G2	G431
1Ch	G225	G208	G18	G415
1Dh	G233	G200	G34	G399

1Eh	G241	G192	G50	G383
1Fh	G249	G184	G66	G367
20h	G257	G176	G82	G351
21h	G265	G168	G98	G335
22h	G273	G160	G114	G319
23h	G281	G152	G130	G303
24h	G289	G144	G146	G287
25h	G297	G136	G162	G271
26h	G305	G128	G178	G255
27h	G313	G120	G194	G239
28h	G321	G112	G210	G223
29h	G329	G104	G226	G207
2Ah	G337	G96	G242	G191
2Bh	G345	G88	G258	G175
2Ch	G353	G80	G274	G159
2Dh	G361	G72	G290	G143
2Eh	G369	G64	G306	G127
2Fh	G377	G56	G322	G111
30h	G385	G48	G338	G95
31h	G393	G40	G354	G79
32h	G401	G32	G370	G63
33h	G409	G24	G386	G47
34h	G417	G16	G402	G31
35h	G425	G8	G418	G15
others	Setting disabled	Setting disabled	Setting disabled	Setting disabled

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line
00h	8
01h	16
02h	24
03h	32
04h	40
05h	48
06h	56
07h	64
08h	72
09h	80
0Ah	88
0Bh	96
0Ch	104
0Dh	112
0Eh	120
0Fh	128
10h	136
11h	144
12h	152

NL[5:0]	LCD Drive Line
13h	160
14h	168
15h	176
16h	184
17h	192
18h	200
19h	208
1Ah	216
1Bh	224
1Ch	232
1Dh	240
1Eh	248
1Fh	256
20h	264
21h	272
22h	280
23h	288
24h	296
25h	304

NL[5:0]	LCD Drive Line
26h	312
27h	320
28h	328
29h	336
2Ah	344
2Bh	352
2Ch	360
2Dh	368
2Eh	376
2Fh	384
30h	392
31h	400
32h	408
33h	416
34h	424
35h	432
others	setting disabled

NDL: Sets the source driver output level in the non-display area.

NDL	Non-Display Area	
	Positive Polarity	Negative Polarity
0	V63	V0
1	V0	V63

GS: Sets the direction of scan by the gate driver in the range determined by SCN[4:0] and NL[4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

When GS = 0, the scan direction is from G1 to G432.

When GS = 1, the scan direction is from G432 to G1

REV: Enables the grayscale inversion of the image by setting REV=1.

REV	GRAM Data	Source Output in Display Area	
		Positive polarity	negative polarity
0	18'h00000	V63	V0
	.	.	.
	.	.	.
	.	.	.
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	.	.	.
	.	.	.
	.	.	.
	18'h3FFFF	V63	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the ILI9326 starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

VLE	Base Image Display
0	Fixed
1	Enable Scrolling

VL[8:0]: Sets the scrolling amount of base image. The base image is scrolled in vertical direction and displayed from the line determined by VL[8:0]. Make sure that VL[8:0] $\leqq$432.

8.2.37. Partial Image 1 Display Position (R500h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTD P0[8]	PTD P0[7]	PTD P0[6]	PTD P0[5]	PTD P0[4]	PTD P0[3]	PTD P0[2]	PTD P0[1]	PTD P0[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP0[8:0]: Sets the display position of partial image 1. The display areas of the partial images 1 and 2 must not overlap each another.

8.2.38. Partial Image 1 RAM Start/End Address (R501h, R502h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R501h	W	1	0	0	0	0	0	0	0	PTS A0[8]	PTS A0[7]	PTS A0[6]	PTS A0[5]	PTS A0[4]	PTS A0[3]	PTS A0[2]	PTS A0[1]	PTS A0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R502h	W	1	0	0	0	0	0	0	0	PTE A0[8]	PTE A0[7]	PTE A0[6]	PTE A0[5]	PTE A0[4]	PTE A0[3]	PTE A0[2]	PTE A0[1]	PTE A0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTSA0[8:0] PTEA0[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 1. Make sure PTSA0[8:0] ≤ PTEA0[8:0].

8.2.39. Partial Image 2 Display Position (R503h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTS A1[8]	PTD P1[7]	PTD P1[6]	PTD P1[5]	PTD P1[4]	PTD P1[3]	PTD P1[2]	PTD P1[1]	PTD P1[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP1[8:0]: Sets the display position of partial image 2 The display areas of the partial images 1 and 2 must not overlap each another.

8.2.40. Partial Image 2 RAM Start/End Address (R504h, R505h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R504h	W	1	0	0	0	0	0	0	0	PTS A1[8]	PTS A1[7]	PTS A1[6]	PTS A1[5]	PTS A1[4]	PTS A1[3]	PTS A1[2]	PTS A1[1]	PTS A1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R505h	W	1	0	0	0	0	0	0	0	PTE A1[8]	PTE A1[7]	PTE A1[6]	PTE A1[5]	PTE A1[4]	PTE A1[3]	PTE A1[2]	PTE A1[1]	PTE A1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

8.2.41. Software Reset (R600h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SRST
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRST When SRST=1, software is reset.

When SRST=0, software reset is canceled.

8.2.42. i80-I/F Endian Control (R606h)

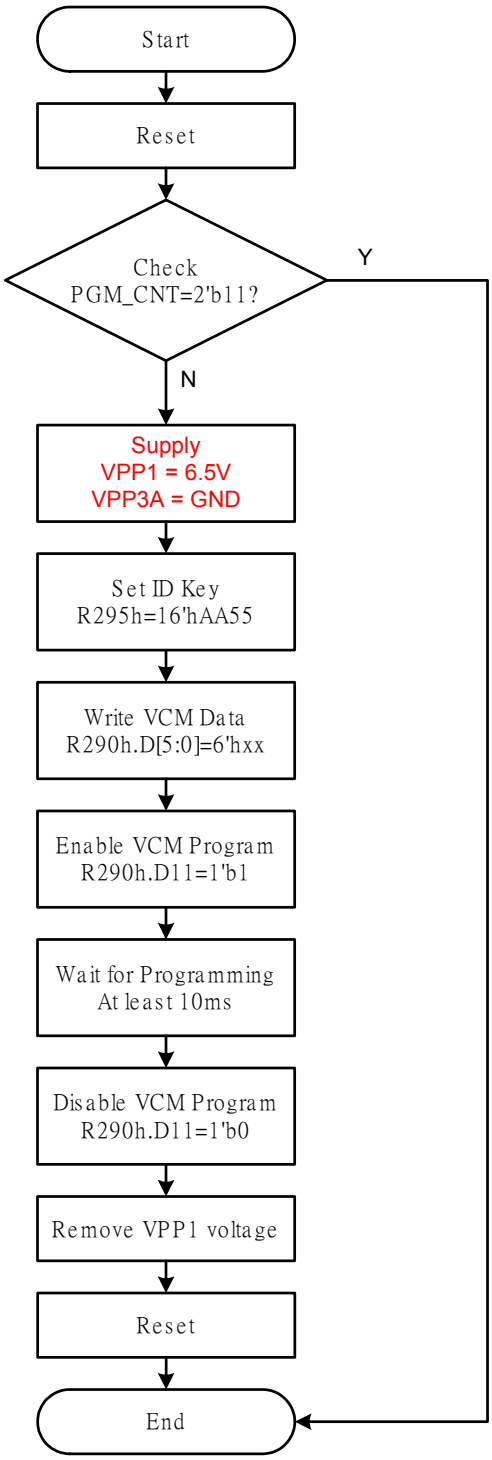
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	TCREV1	0	0	0	0	0	0	0	TCREV0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TCREV[1:0]: Control the endian setting (big/little endian: order of receiving data) when transferring one-pixel data via i80 interface.

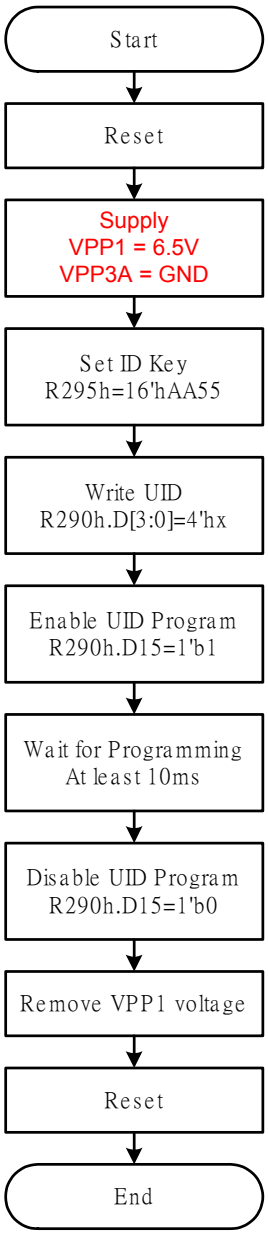
TCREV[1:0]	2 transfer/pixel	3 transfer/pixel
00	Upper to low (1^{st} to 2^{nd})	Upper to low (1^{st} , 2^{nd}, 3^{rd})
01	Setting disable	Setting disable
10	Setting disable	Setting disable
11	Low to upper (2^{nd} to 1^{st})	Low to upper (3^{rd} , 2^{nd} , 1^{st})

9. MTP Programming Flow

VCOMH OTP programming Flow



UID OTP programming Flow



10. GRAM Address Map & Read/Write

ILI9326 has an internal graphics RAM (GRAM) of 233,280 bytes to store the display data and one pixel is constructed of 18 bits. The GRAM can be accessed through the i80 system, SPI and RGB interfaces.

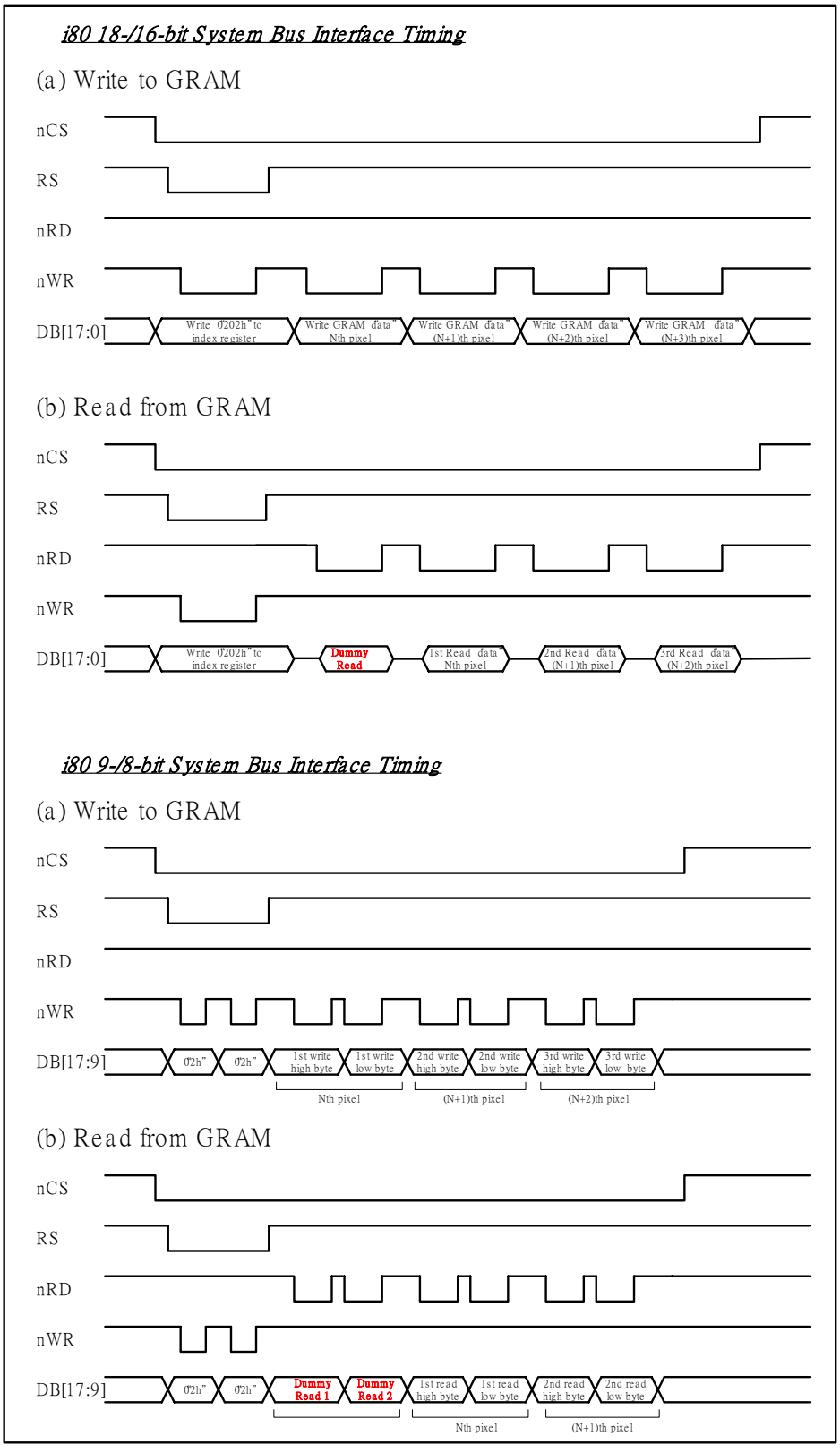
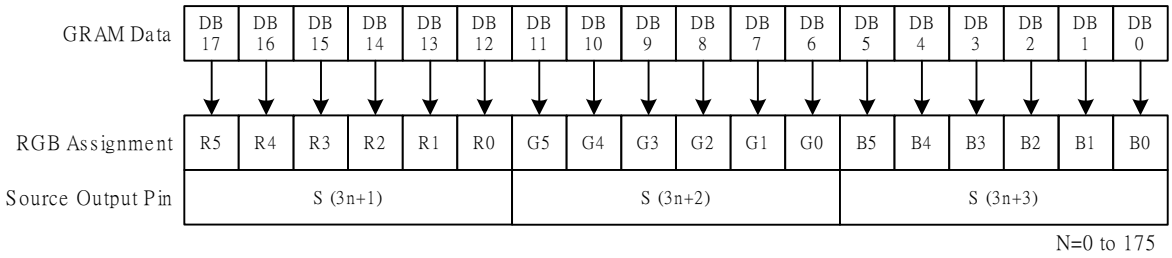


Figure31 GRAM Read/Write Timing of i80-System Interface

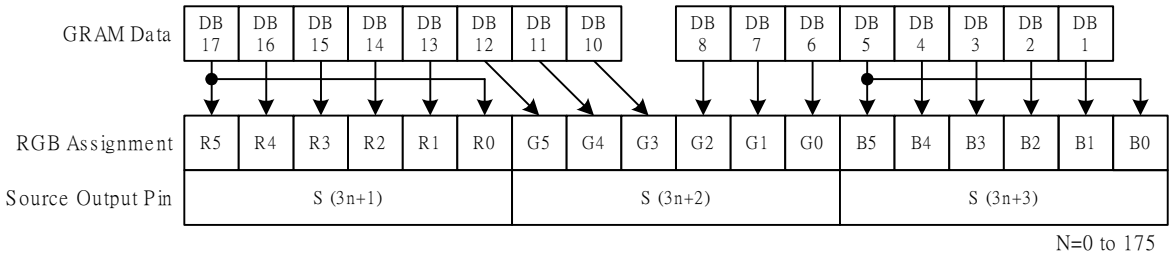
GRAM address map table of SS=0, BGR=0

SS=0, BGR=0		S1…S3	S4…S6	S7…S9	S10…S12	…	S517…S519	S520…S522	S523…S525	S526…S720
GS=0	**GS=1**	DB17…0	DB17…0	DB17…0	DB17…0	…	DB17…0	DB17…0	DB17…0	DB17…0
G1	G432	“00000h”	“00001h”	“00002h”	“00003h”	…	“000ECh”	“000EDh”	“000EEh”	“000EFh”
G2	G431	“00100h”	“00101h”	“00102h”	“00103h”	…	“001ECh”	“001EDh”	“001EEh”	“001EFh”
G3	G430	“00200h”	“00201h”	“00202h”	“00203h”	…	“002ECh”	“002EDh”	“002EEh”	“002EFh”
G4	G429	“00300h”	“00301h”	“00302h”	“00303h”	…	“003ECh”	“003EDh”	“003EEh”	“003EFh”
G5	G428	“00400h”	“00401h”	“00402h”	“00403h”	…	“004ECh”	“004EDh”	“004EEh”	“004EFh”
G6	G427	“00500h”	“00501h”	“00502h”	“00503h”	…	“005ECh”	“005EDh”	“005EEh”	“005EFh”
G7	G426	“00600h”	“00601h”	“00602h”	“00603h”	…	“006ECh”	“006EDh”	“006EEh”	“006EFh”
G8	G425	“00700h”	“00701h”	“00702h”	“00703h”	…	“007ECh”	“007EDh”	“007EEh”	“007EFh”
G9	G424	“00800h”	“00801h”	“00802h”	“00803h”	…	“008ECh”	“008EDh”	“008EEh”	“008EFh”
G10	G423	“00900h”	“00901h”	“00902h”	“00903h”	…	“009ECh”	“009EDh”	“009EEh”	“009EFh”
. . .	. . .	. . .	. . .	. . .	. . .	…	. . .	. . .	. . .	. . .
G423	G10	“1A600h”	“1A601h”	“1A602h”	“1A603h”	…	“1A6ECh”	“1A6EDh”	“1A6EEh”	“1A6EFh”
G424	G9	“1A700h”	“1A701h”	“1A702h”	“1A703h”	…	“1A7ECh”	“1A7EDh”	“1A7EEh”	“1A7EFh”
G425	G8	“1A800h”	“1A801h”	“1A802h”	“1A803h”	…	“1A8ECh”	“1A8EDh”	“1A8EEh”	“1A8EFh”
G426	G7	“1A900h”	“1A901h”	“1A902h”	“1A903h”	…	“1A9ECh”	“1A9EDh”	“1A9EEh”	“1A9EFh”
G427	G6	“1AA00h”	“1AA01h”	“1AA02h”	“1AA03h”	…	“1AAECh”	“1AAEDh”	“1AAEEh”	“1AAEFh”
G428	G5	“1AB00h”	“1AB01h”	“1AB02h”	“1AB03h”	…	“1ABECh”	“1ABEDh”	“1ABEEh”	“1ABEFh”
G429	G4	“1AC00h”	“1AC01h”	“1AC02h”	“1AC03h”	…	“1ACECh”	“1ACEDh”	“1ACEEh”	“1ACEFh”
G430	G3	“1AD00h”	“1AD01h”	“1AD02h”	“1AD03h”	…	“1ADECh”	“1ADEDh”	“1ADEEh”	“1ADEFh”
G431	G2	“1AE00h”	“1AE01h”	“1AE02h”	“1AE03h”	…	“1AEECh”	“1AEEDh”	“1AEEEh”	“1AEEFh”
G432	G1	“1AF00h”	“1AF01h”	“1AF02h”	“1AF03h”	…	“1AFECh”	“1AFEDh”	“1AFEEh”	“1AFEFh”

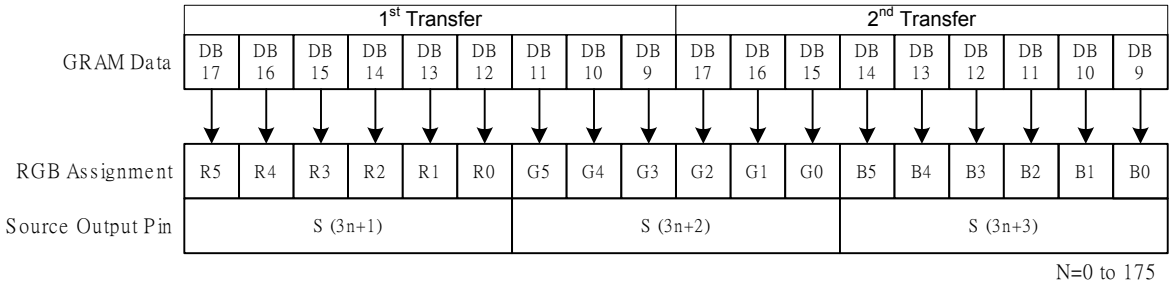
i80/M68 system 18-bit data bus interface



i80/M68 system 16-bit data bus interface



i80/M68 system 9-bit data bus interface



GRAM Data and display data of 18-/16-/9-bit system interface (SS="0", BGR="0")

Figure32 i80-System Interface with 18-/16-/9-bit Data Bus (SS="0", BGR="0")

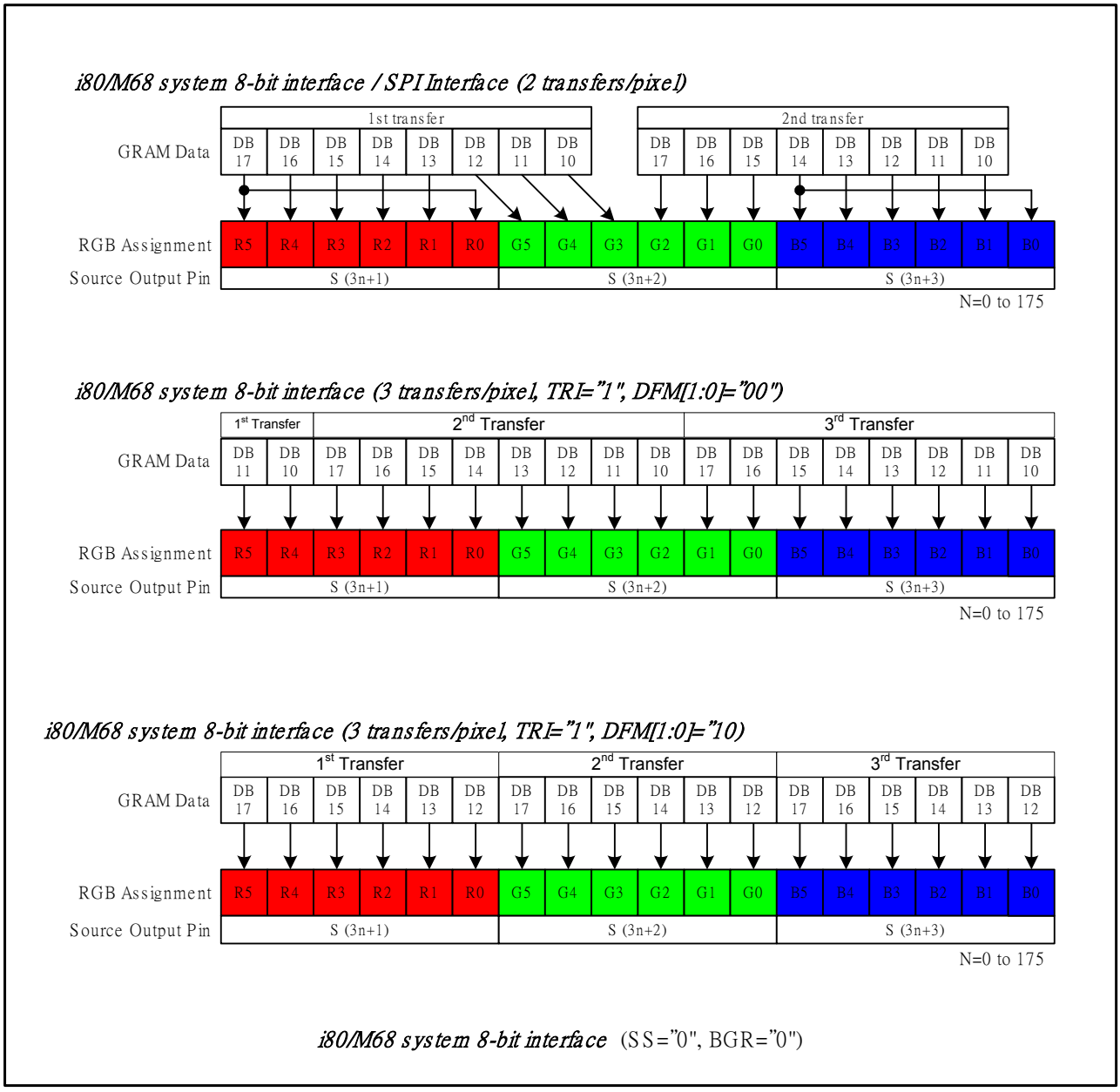


Figure33 i80-System Interface with 8-bit Data Bus (SS="0", BGR="0")

GRAM address map table of SS=1, BGR=1

SS=0, BGR=0		S720…S718	S717…S715	S714…S712	S711…S709	…	S12…S10	S9…S7	S6…S4	S3…S1
GS=0	**GS=1**	DB17…0	DB17…0	DB17…0	DB17…0	…	DB17…0	DB17…0	DB17…0	DB17…0
G1	G432	“00000h”	“00001h”	“00002h”	“00003h”	…	“000ECh”	“000EDh”	“000EEh”	“000EFh”
G2	G431	“00100h”	“00101h”	“00102h”	“00103h”	…	“001ECh”	“001EDh”	“001EEh”	“001EFh”
G3	G430	“00200h”	“00201h”	“00202h”	“00203h”	…	“002ECh”	“002EDh”	“002EEh”	“002EFh”
G4	G429	“00300h”	“00301h”	“00302h”	“00303h”	…	“003ECh”	“003EDh”	“003EEh”	“003EFh”
G5	G428	“00400h”	“00401h”	“00402h”	“00403h”	…	“004ECh”	“004EDh”	“004EEh”	“004EFh”
G6	G427	“00500h”	“00501h”	“00502h”	“00503h”	…	“005ECh”	“005EDh”	“005EEh”	“005EFh”
G7	G426	“00600h”	“00601h”	“00602h”	“00603h”	…	“006ECh”	“006EDh”	“006EEh”	“006EFh”
G8	G425	“00700h”	“00701h”	“00702h”	“00703h”	…	“007ECh”	“007EDh”	“007EEh”	“007EFh”
G9	G424	“00800h”	“00801h”	“00802h”	“00803h”	…	“008ECh”	“008EDh”	“008EEh”	“008EFh”
G10	G423	“00900h”	“00901h”	“00902h”	“00903h”	…	“009ECh”	“009EDh”	“009EEh”	“009EFh”
. . .	. . .	. . .	. . .	. . .	. . .	…	. . .	. . .	. . .	. . .
G423	G10	“1A600h”	“1A601h”	“1A602h”	“1A603h”	…	“1A6ECh”	“1A6EDh”	“1A6EEh”	“1A6EFh”
G424	G9	“1A700h”	“1A701h”	“1A702h”	“1A703h”	…	“1A7ECh”	“1A7EDh”	“1A7EEh”	“1A7EFh”
G425	G8	“1A800h”	“1A801h”	“1A802h”	“1A803h”	…	“1A8ECh”	“1A8EDh”	“1A8EEh”	“1A8EFh”
G426	G7	“1A900h”	“1A901h”	“1A902h”	“1A903h”	…	“1A9ECh”	“1A9EDh”	“1A9EEh”	“1A9EFh”
G427	G6	“1AA00h”	“1AA01h”	“1AA02h”	“1AA03h”	…	“1AAECh”	“1AAEDh”	“1AAEEh”	“1AAEFh”
G428	G5	“1AB00h”	“1AB01h”	“1AB02h”	“1AB03h”	…	“1ABECh”	“1ABEDh”	“1ABEEh”	“1ABEFh”
G429	G4	“1AC00h”	“1AC01h”	“1AC02h”	“1AC03h”	…	“1ACECh”	“1ACEDh”	“1ACEEh”	“1ACEFh”
G430	G3	“1AD00h”	“1AD01h”	“1AD02h”	“1AD03h”	…	“1ADECh”	“1ADEDh”	“1ADEEh”	“1ADEFh”
G431	G2	“1AE00h”	“1AE01h”	“1AE02h”	“1AE03h”	…	“1AEECh”	“1AEEDh”	“1AEEEh”	“1AEEFh”
G432	G1	“1AF00h”	“1AF01h”	“1AF02h”	“1AF03h”	…	“1AFECh”	“1AFEDh”	“1AFEEh”	“1AFEFh”

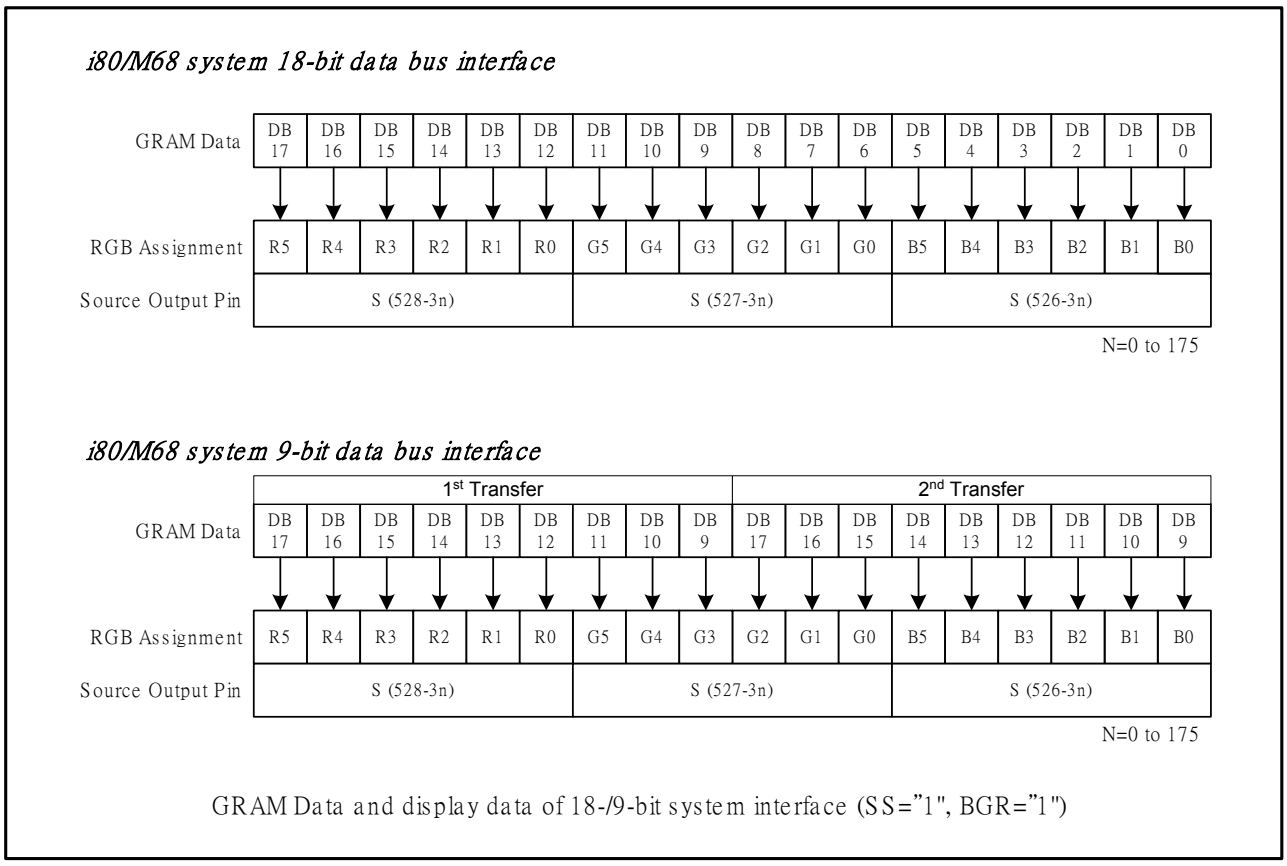


Figure 34 i80-System Interface with 18-/9-bit Data Bus (SS="1", BGR="1")

11. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA[7:0], end: HEA[7:0] bits) and the vertical address register (start: VSA[8:0], end: VEA[8:0] bits). The AM bit sets the transition direction of RAM address (either increment or decrement). These bits enable the ILI9326 to write data including image data consecutively not taking data wrap positions into account.

The window address area must be made within the GRAM address map area. Also, the GRAM address bits (RAM address set register) must be an address within the window address area.

[Window address setting area]

(Horizontal direction) 00H ≤ HSA[7:0] ≤ HEA[7:0] ≤ "EF"H

(Vertical direction) 00H ≤ VSA[8:0] ≤ VEA[8:0]≤ "13F"H

[RAM address, AD (an address within a window address area)]]

(RAM address) HSA[7:0] ≤ AD[7:0] ≤ HEA[7:0]

VSA[8:0] ≤ AD[15:8] ≤ VEA[8:0]

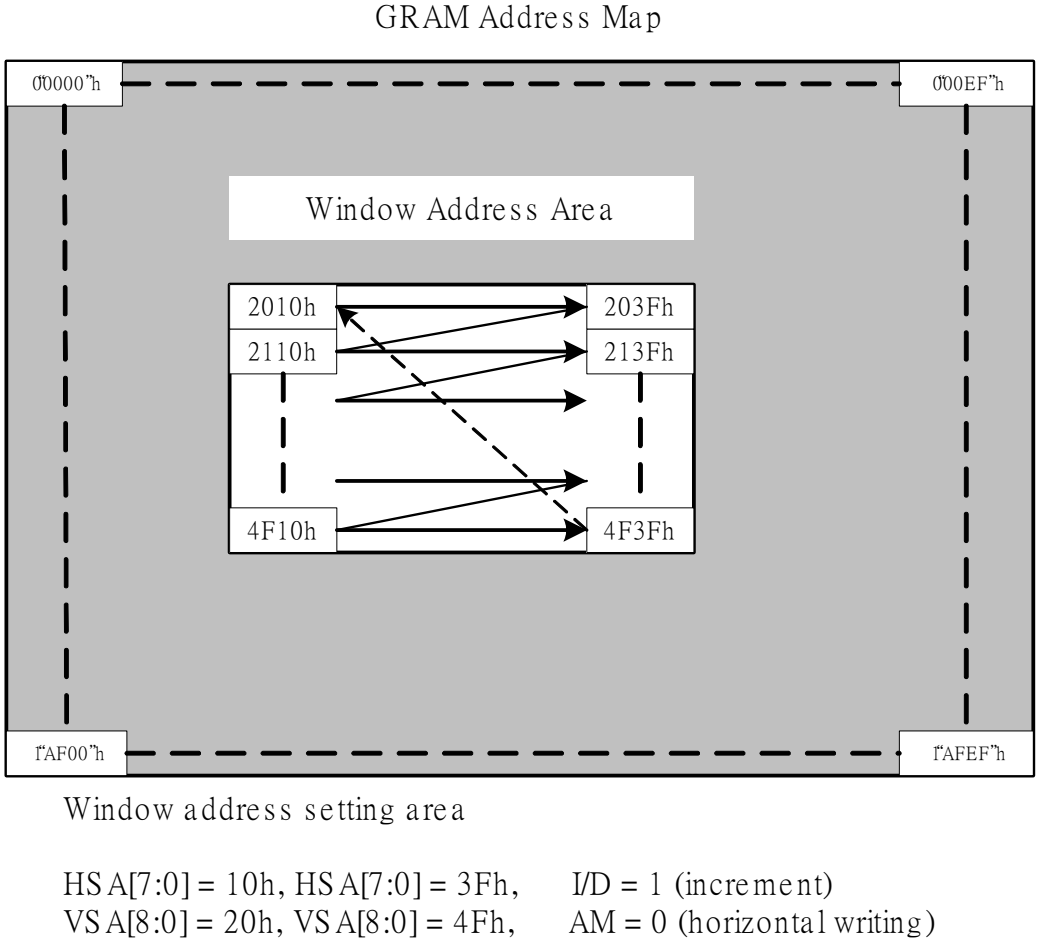


Figure 35 GRAM Access Window Map

12. Gamma Correction

ILI9326 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make ILI9326 available with liquid crystal panels of various characteristics.

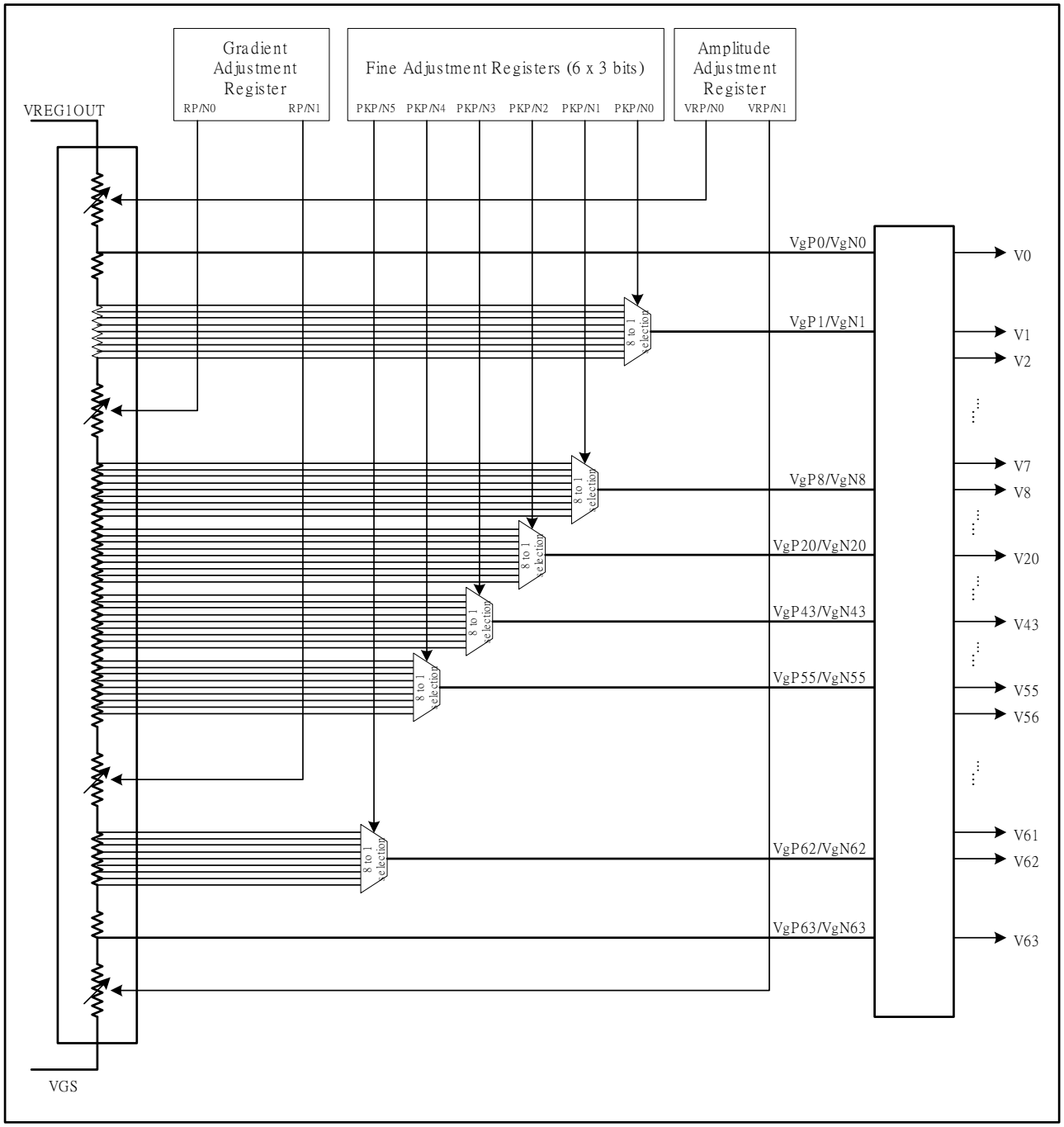


Figure 36 Grayscale Voltage Generation

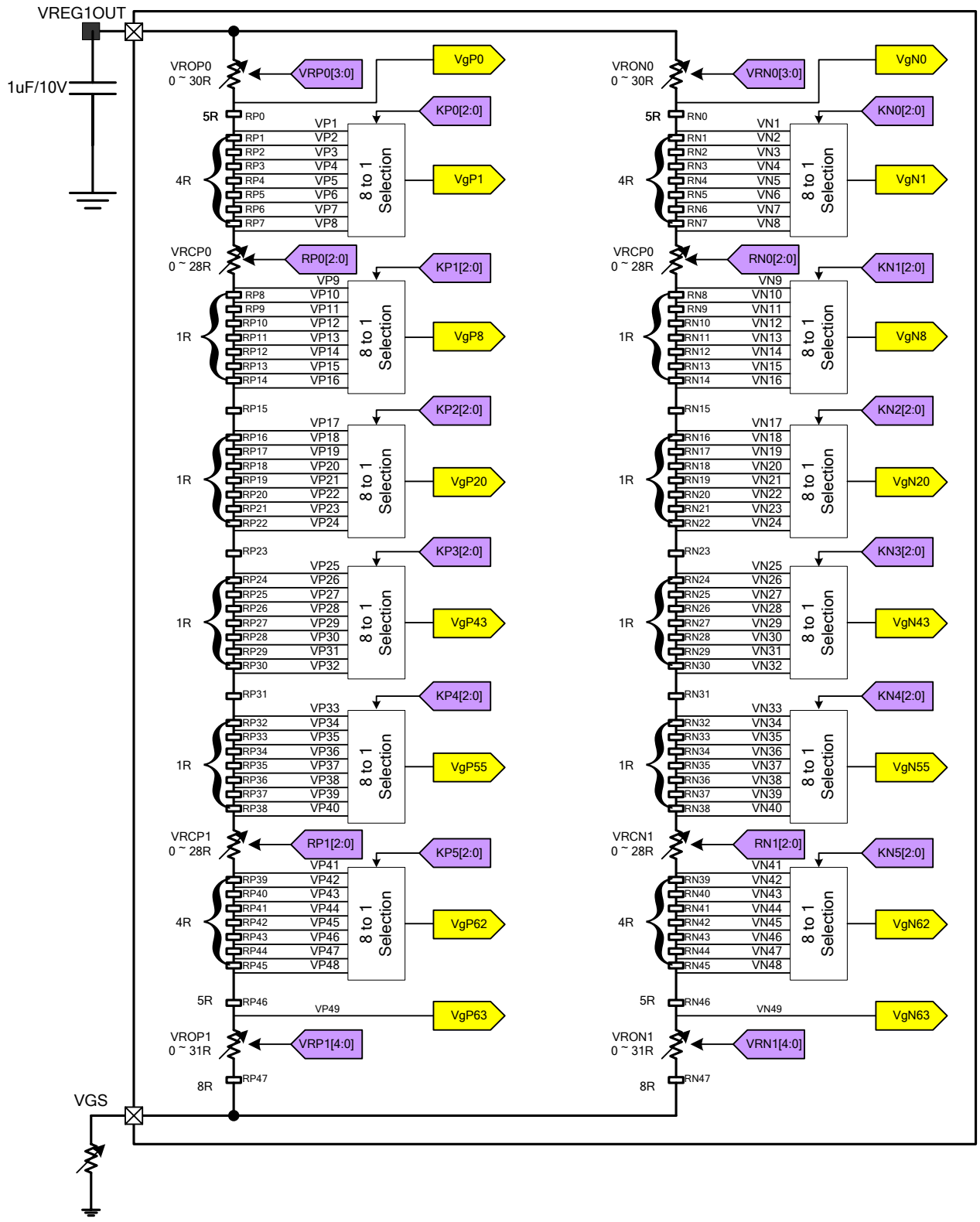


Figure 37 Grayscale Voltage Adjustment

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers RP0[2:0]/RN0[2:0], RP1[2:0]/RN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers, VRP0[4:0]/VRN0[4:0], VRP1[4:0]/VRN1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

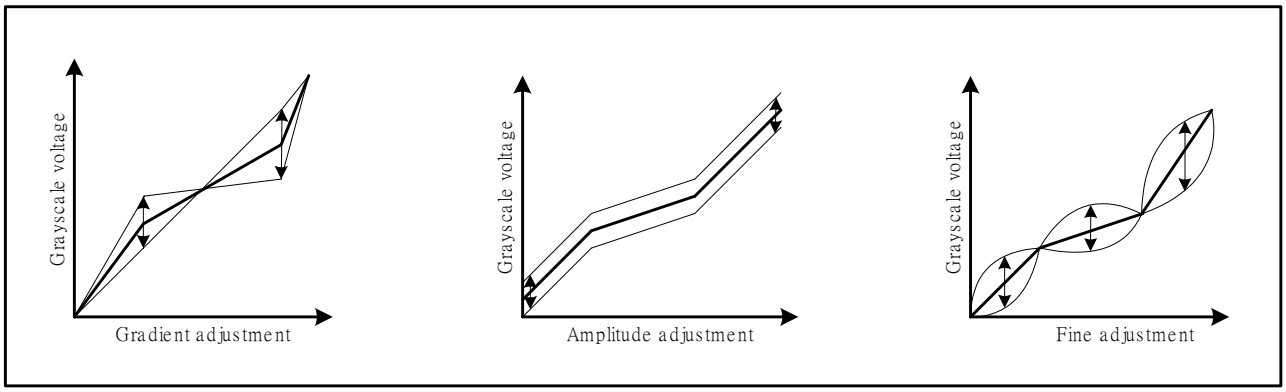


Figure 38 Gamma Curve Adjustment

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	RP0 [2:0]	RN0 [2:0]	Variable resistor VRCP0, VRCN0
	RP1 [2:0]	RN1 [2:0]	Variable resistor VRCP1, VRCN1
Amplitude adjustment	VRP0 [3:0]	VRN0 [3:0]	Variable resistor VROP0, VRON0
	VRP1 [4:0]	VRN1 [4:0]	Variable resistor VROP1, VRON1
Fine adjustment	KP0 [2:0]	KN0 [2:0]	8-to-1 selector (voltage level of grayscale 1)
	KP1 [2:0]	KN1 [2:0]	8-to-1 selector (voltage level of grayscale 8)
	KP2 [2:0]	KN2 [2:0]	8-to-1 selector (voltage level of grayscale 20)
	KP3 [2:0]	KN3 [2:0]	8-to-1 selector (voltage level of grayscale 43)
	KP4 [2:0]	KN4 [2:0]	8-to-1 selector (voltage level of grayscale 55)
	KP5 [2:0]	KN5 [2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8-to-1 selector Block configuration

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the **γ-**correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Fine adjustment registers and selected voltage

Register	Selected Voltage					
KP(N)[2:0]	VgP(N)1	VgP(N)8	VgP(N)20	VgP(N)43	VgP(N)55	VgP(N)62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

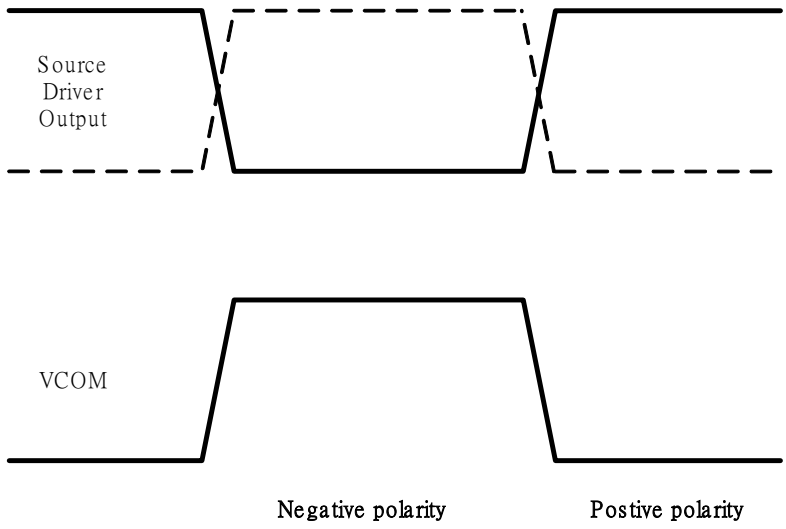


Figure 39 Relationship between Source Output and VCOM

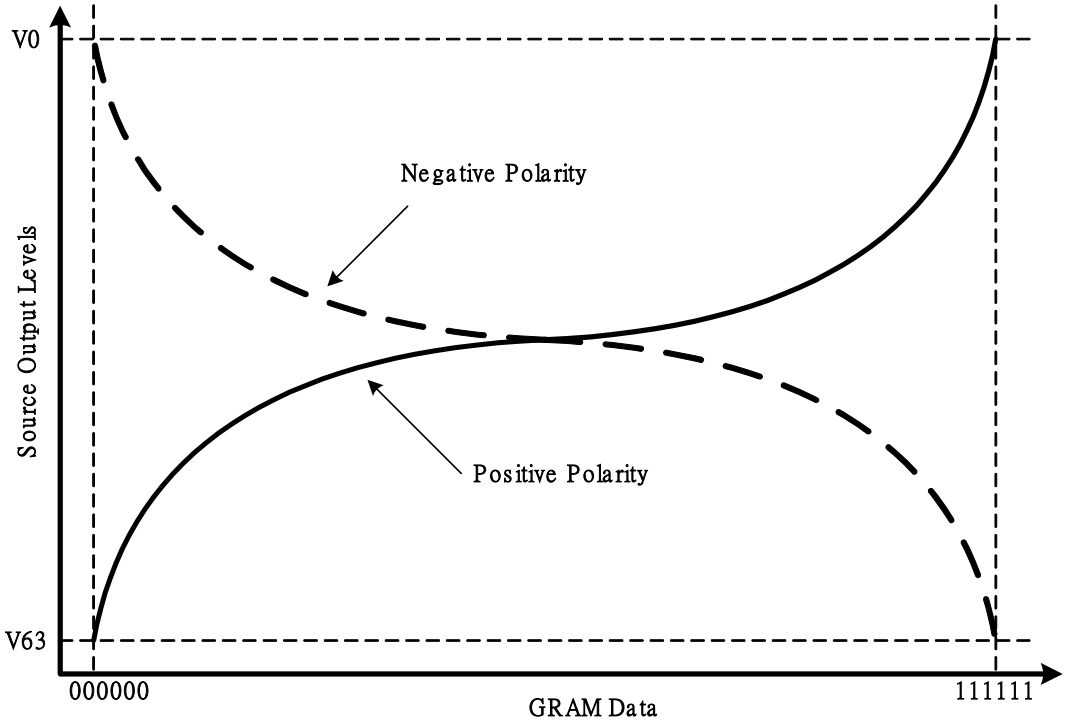


Figure 40 Relationship between GRAM Data and Output Level

13. Application

13.1. Configuration of Power Supply Circuit

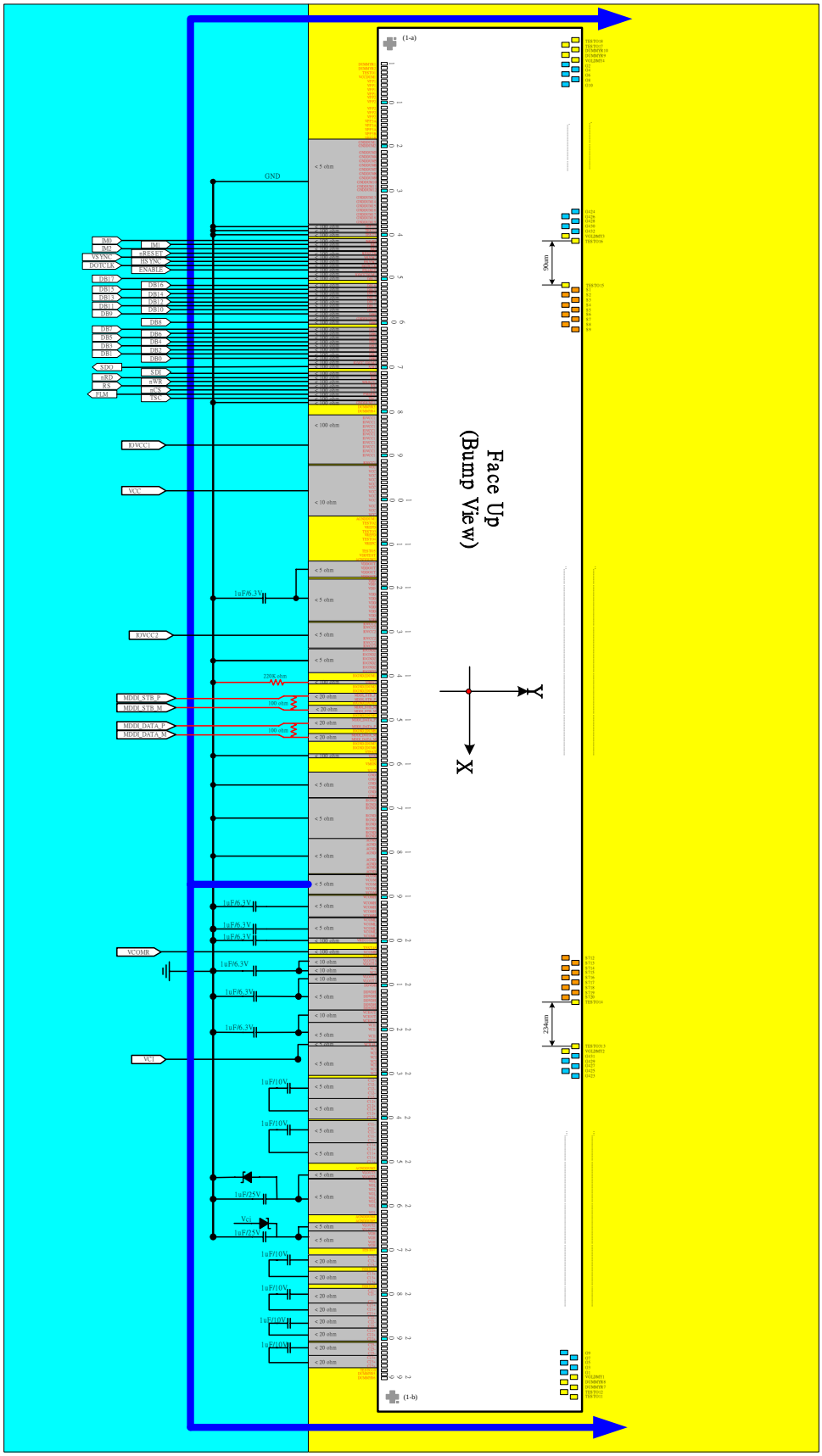


Figure 41 Power Supply Circuit Block

The following table shows specifications of external elements connected to the ILI9326's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 μF (B characteristics)	6.3V	VREG1OUT, VCI1, VDD, VCL, VCOMH, VCOML, C11+/-, C12+/-, C13+/-
	10V	DDVDH, C21+/-, C22+/-, C23+/-
	25V	VGH, VGL
Schottky diode	**VF<0.4V/20mA at 25°C, VR ≥30V (Recommended diode: HSC226)**	**(AGND – VGL), (Vci – VGH), (Vci – DDVDH)**

13.2. Display ON/OFF Sequence

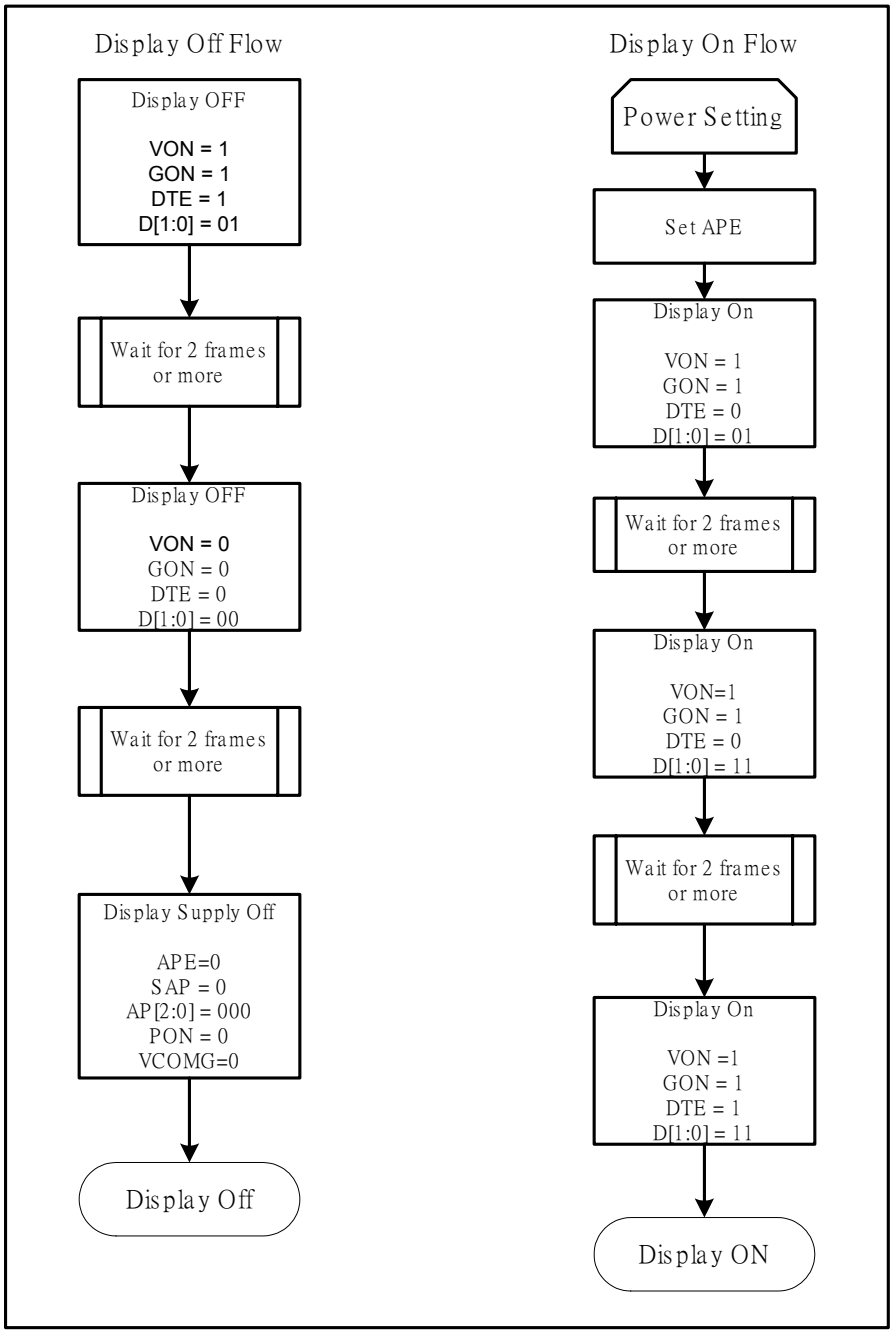


Figure 42 Display On/Off Register Setting Sequence

13.3. Standby and Sleep Mode

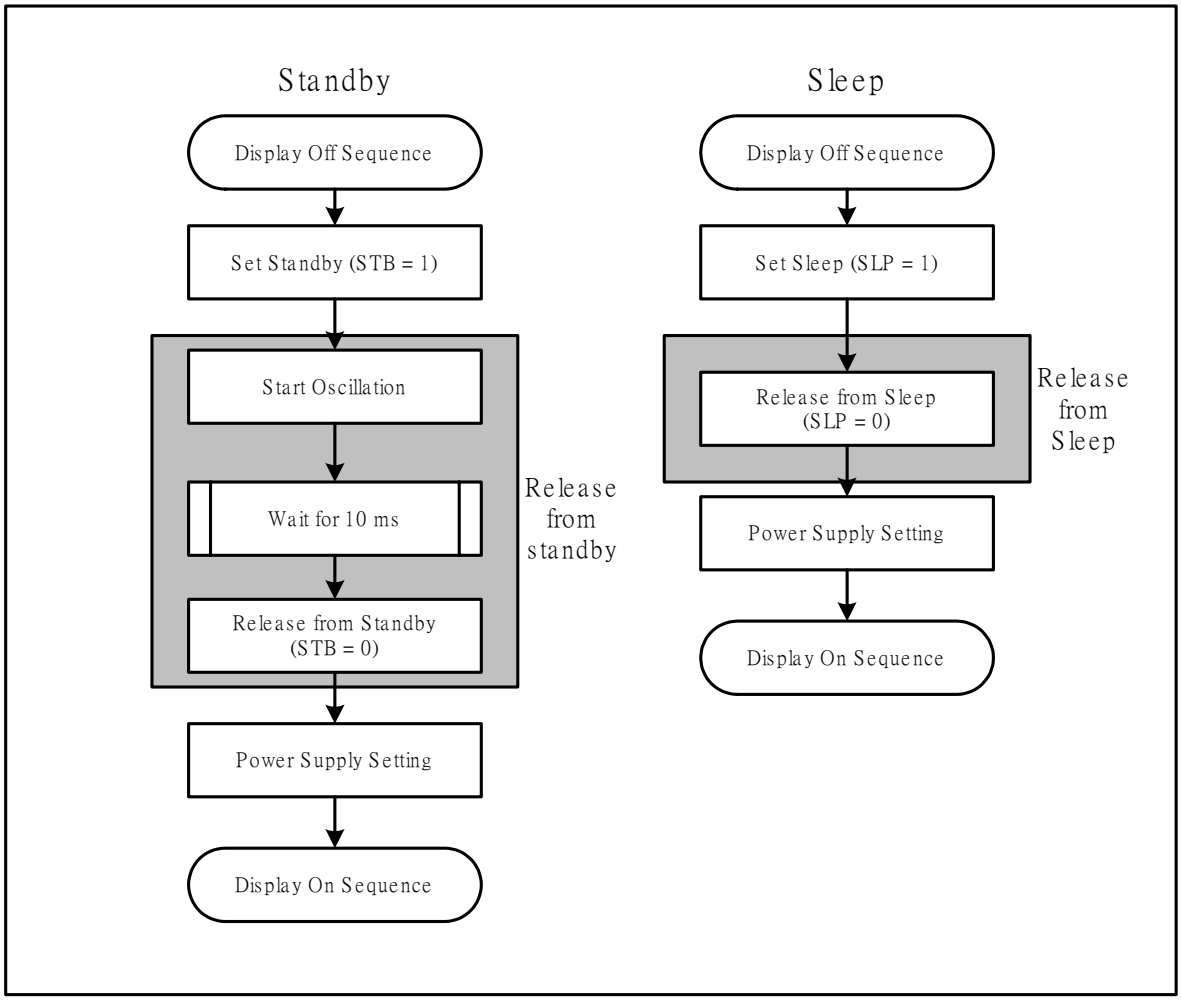


Figure 43 Standby/Sleep Mode Register Setting Sequence

13.4. Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.

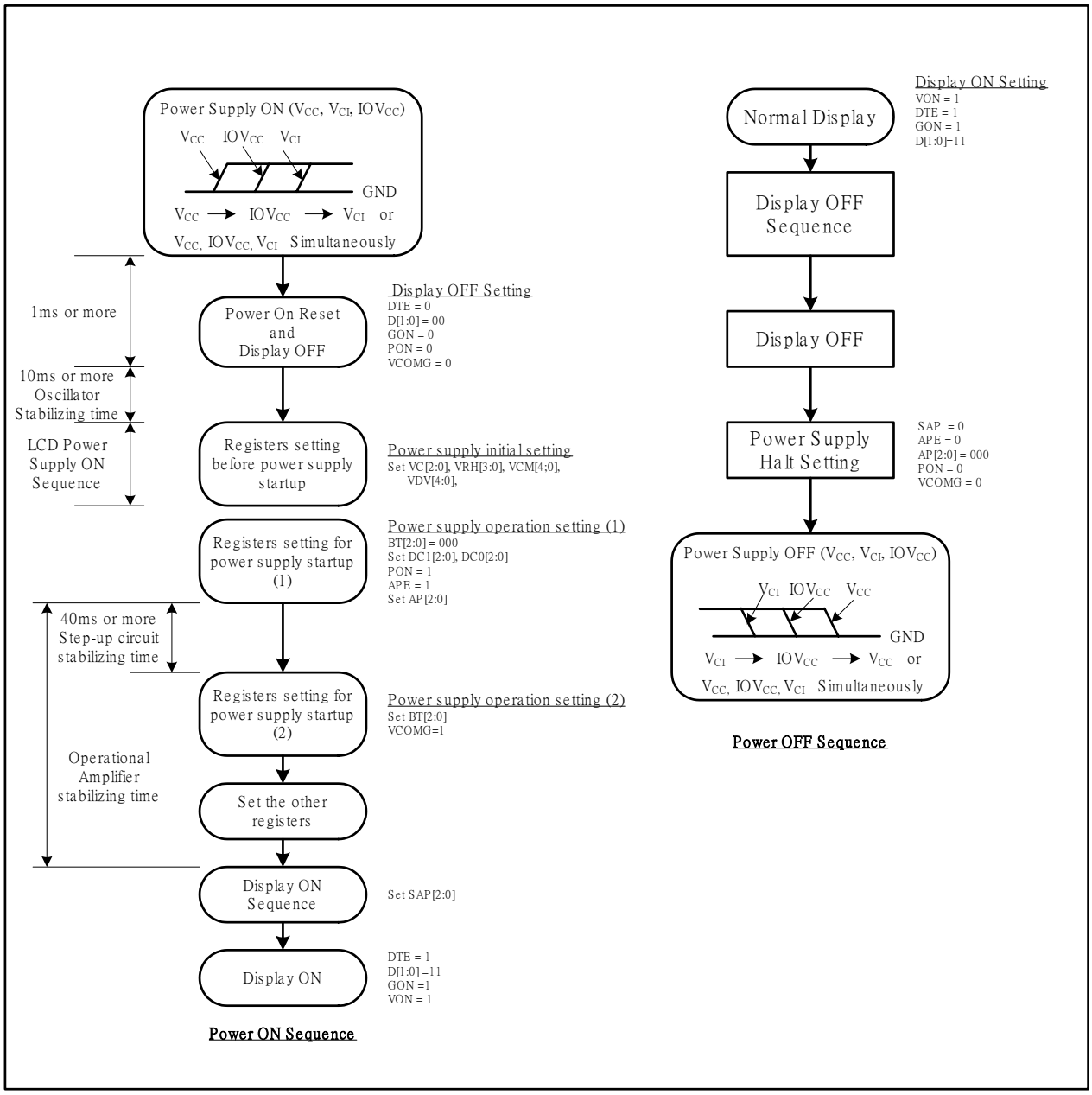


Figure 44 Power Supply ON/OFF Sequence

13.5. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the ILI9326 are as follows.

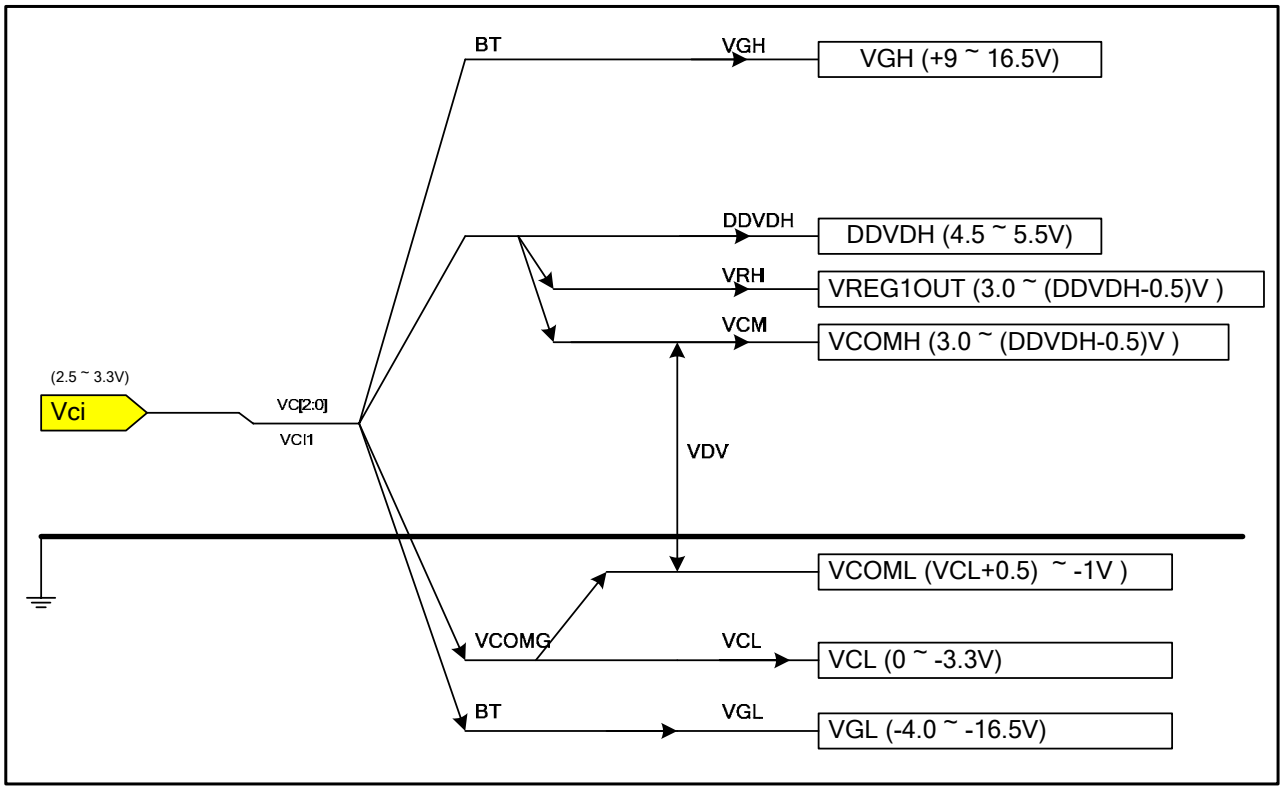


Figure 45 Voltage Configuration Diagram

Note: The DDVDH, VGH, VGL, and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to current consumption at respective outputs. The voltage levels in the following relationships (DDVDH – VREG1OUT) > 0.5V, (VCOML – VCL) > 0.5V, (VCOML – VCL) > 0.5V are the actual voltage levels. When the alternating cycles of VCOM are set high (e.g. the polarity inverts every line cycle), current consumption is large. In this case, check the voltage before use.

13.6. Applied Voltage to the TFT panel

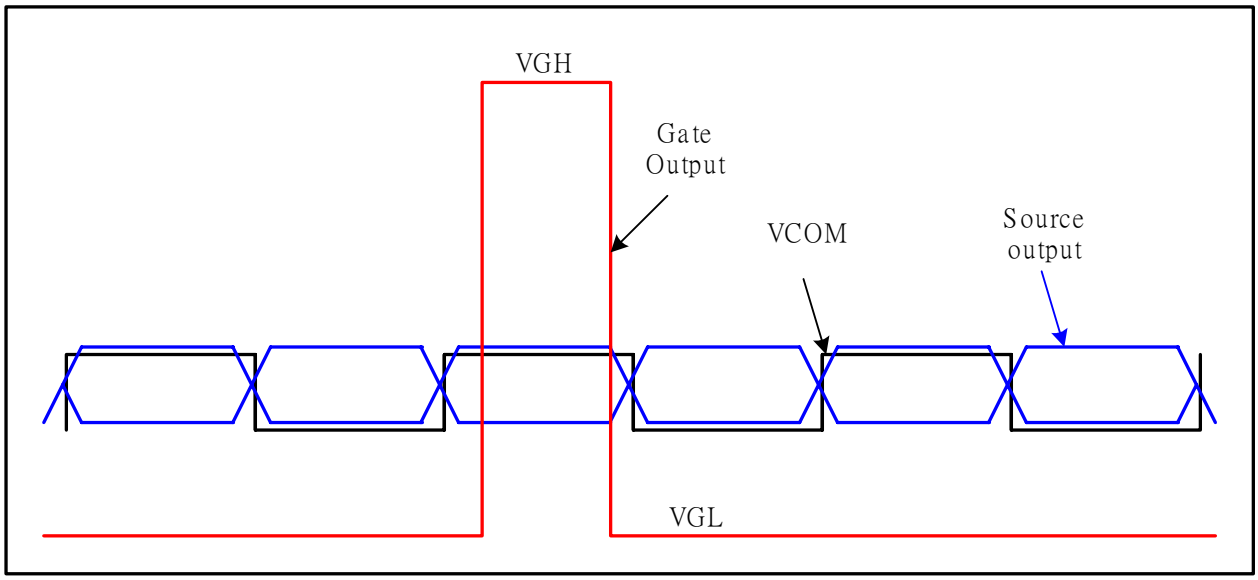


Figure 46 Voltage Output to TFT LCD Panel

13.7. Partial Display Function

The ILI9326 allows selectively driving two partial images on the screen at arbitrary positions set in the screen drive position registers.

The following example shows the setting for partial display function:

Base Image Display Setting	
BASEE	**0**
NL[5:0]	**6'h27**
Partial Image 1 Display Setting	
PTDE0	**1**
PTSA0[8:0]	**9'h000**
PTEA0[8:0]	**9'h00F**
PTDP0[8:0]	**9'h080**
Partial Image 2 Display Setting	
PTDE1	**1**
PTSA1[8:0]	**9'h020**
PTEA1[8:0]	**9'h02F**
PTDP1[8:0]	**9'h0C0**

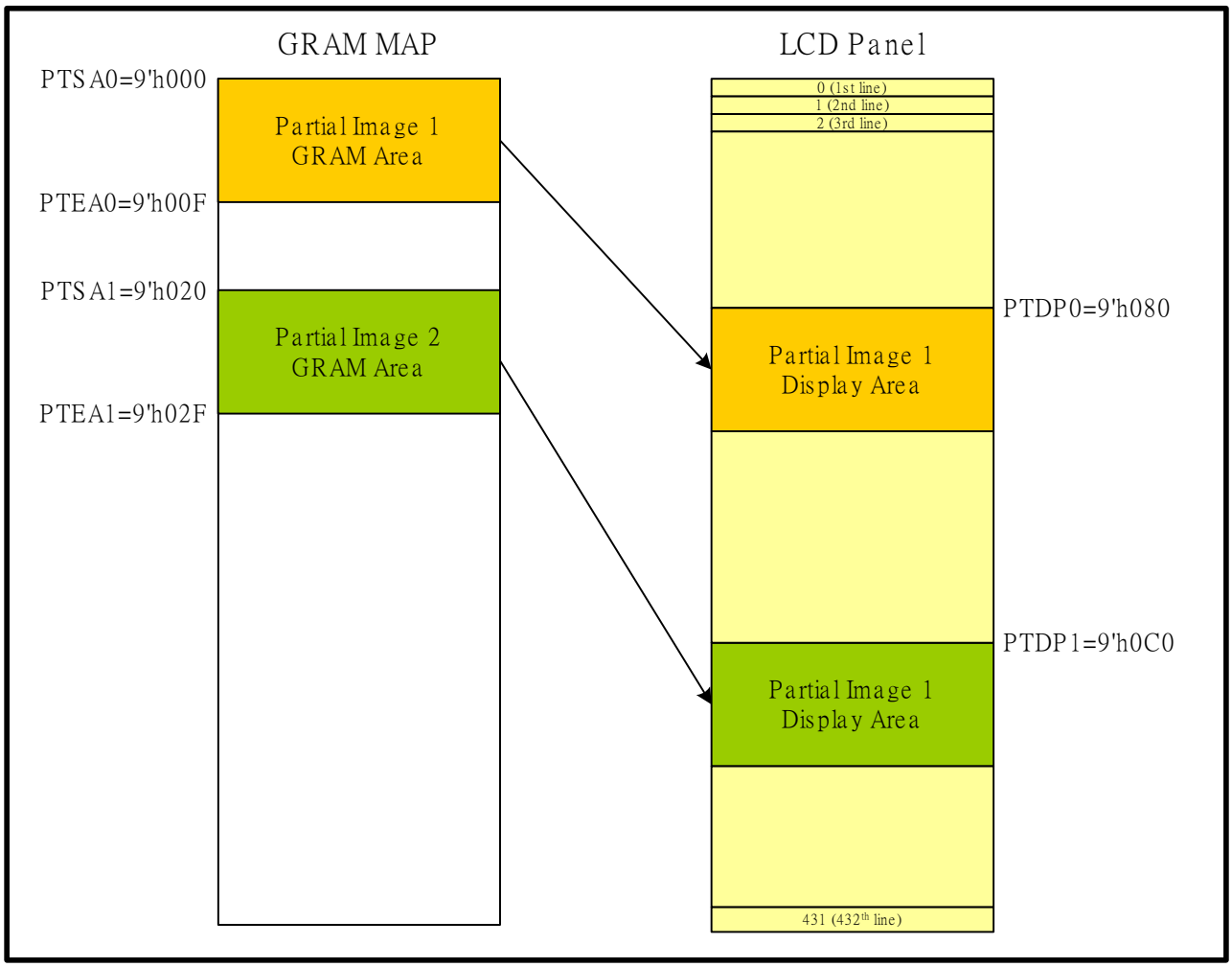


Figure 47 Partial Display Example

14. Electrical Characteristics

14.1. Absolute Maximum Ratings

The absolute maximum rating is listed in following table. When ILI9326 is used out of the absolute maximum ratings, ILI9326 may be permanently damaged. To use ILI9326 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9326 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	VCC, IOVCC1, IOVCC2	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (1)	VCI - AGND	V	-0.3 ~ + 4.6	1, 4
Power supply voltage (1)	DDVDH - AGND	V	-0.3 ~ + 6.0	1, 4
Power supply voltage (1)	AGND -VCL	V	-0.3 ~ + 4.6	1
Power supply voltage (1)	DDVDH - VCL	V	-0.3 ~ + 9.0	1, 5
Power supply voltage (1)	VGH - AGND	V	-0.3 ~ + 18.5	1, 5
Power supply voltage (1)	AGND - VGL	V	-0.3 ~ + 18.5	1, 6
Input voltage	Vt	V	-0.3 ~ VCC+ 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	8, 9
Storage temperature	Tstg	°C	-55 ~ + 110	8, 9

Notes:
1. VCC,GND must be maintained
2. (High) (VCC = VCC) ≥ GND (Low), (High) IOVCC1, IOVCC2≥ GND (Low).
3. Make sure (High) VCI ≥ GND (Low).
4. Make sure (High) DDVDH ≥ ASSD (Low).
5. Make sure (High) DDVDH ≥ VCL (Low).
6. Make sure (High) VGH ≥ ASSD (Low).
7. Make sure (High) ASSD ≥ VGL (Low).
8. For die and wafer products, specified up to 85°C.
9. This temperature specifications apply to the TCP package

14.2. DC Characteristics

(VCC = 2.40 ~ 3.30V, IOVCC1 = 1.65 ~ 3.30V, Ta= -40 ~ 85 °C)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	VCC= 2.4~ 3.3V	0.8*IOVCC1	-	IOVCC1	-
Input low voltage	V_{IL}	V	VCC= 2.4 ~ 3.3V	-0.3	-	0.2*IOVCC1	-
Output high voltage(1) (DB0-17 Pins)	V_{OH1}	V	IOH = -0.1 mA	0.8*IOVCC1	-	-	-
Output low voltage (DB0-17 Pins)	V_{OL1}	V	IOVCC1=1.65~3.3V VCC= 2.4 ~ 3.3V IOL = 0.1mA	-	-	0.2*IOVCC1	-
I/O leakage current	I_{LI}	µA	Vin = 0 ~ VCC	-0.1	-	0.1	-
Current consumption during normal operation (V_{CC} – GND)	I_{OP}	µA	VCC=2.8V , Ta=25°C , fOSC = 512KHz (Line) GRAM data = 0000h	-	100 (VCC)	-	-
Current consumption during standby mode (V_{CC} – GND)	I_{ST}	µA	VCC=2.8V , Ta=25 °C	-	5	10	-
LCD Driving Voltage (DDVDH-GND)	DDVDH	V	-	4.5	-	6	-
Output voltage deviation		mV	-	-	5	-	-
Dispersion of the Average Output Voltage	V	mV	-	-10	-	10	-

MDDI DC Characteristics

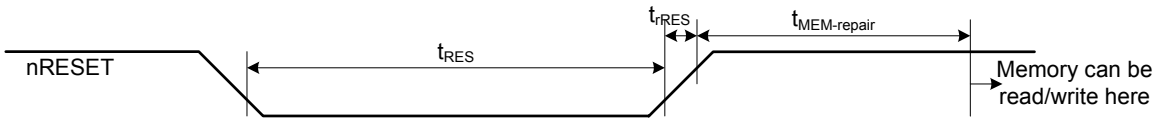
(VCC = IOVCC2=2.50 ~ 3.30V, IOVCC1 = 1.65 ~ 3.30V, Ta= -40 ~ 85 °C)

Items	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Differential input "High" level voltage (VT=0) (MDDI_DATA_P/M, MDDI_STB_P/M)	V_{IT+}	mV		-	0	50	-
Differential input "Low" level voltage (VT=0) (MDDI_DATA_P/M, MDDI_STB_P/M)	V_{IT-}	mV		-50	0	-	-
Differential input "High" level voltage, (VT=125mV) (MDDI_DATA_P/M)	V_{IT+off}	mV		-	125	175	-
Differential input "Low" level voltage (VT=125mV) (MDDI_DATA_P/M)	V_{IT-off}	mV		75	125	-	-
Input voltage range	V_{IRNG}	V		0	-	1.65	-
Current consumption (IOVCC2 - GND) In Hibernation	I_{hib}	uA	IOVCC1=IOVCC2=VCC=2.8V, 1/t BIT=70Mbps, Ta=25℃, DFM=0, offset=0.8V	-	65	100	-
Current consumption (IOVCC2 - GND) In data transfer	I_{trans}	mA	IOVCC1=IOVCC2=VCC=2.8V, in video stream packet transfer, 1/t BIT=70Mbps, Ta=25℃, DFM=0, offset=0.8V	-	0.4 note1	-	-

14.3. Reset Timing Characteristics

Reset Timing Characteristics (VCC = 1.8 ~ 3.3 V, IOVCC1 = 1.65 ~ 3.3 V)

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	t_{RES}	µs	100	-	-
Reset rise time	t_{rRES}	µs	-	-	10
Reset rise time	$t_{MEM-repair}$	ms	50	-	



14.4. AC Characteristics

14.4.1. i80-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.3V, VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	100	-	-	-

	Read	t_{CYCR}	ns	300	-	-	-
Write low-level pulse width		PW_{LW}	ns	50	-	500	-
Write high-level pulse width		PW_{HW}	ns	50	-	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	-	
Write / Read rise / fall time		t_{WRr}/t_{WRf}	ns	-	-	25	
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	-	
	Read (RS to nCS, RW/nRD)			5	-	-	
Address hold time		t_{AH}	ns	5	-	-	
Write data set up time		t_{DSW}	ns	10	-	-	
Write data hold time		t_H	ns	15	-	-	
Read data delay time		t_{DDR}	ns	-	-	100	
Read data hold time		t_{DHR}	ns	5	-	-	

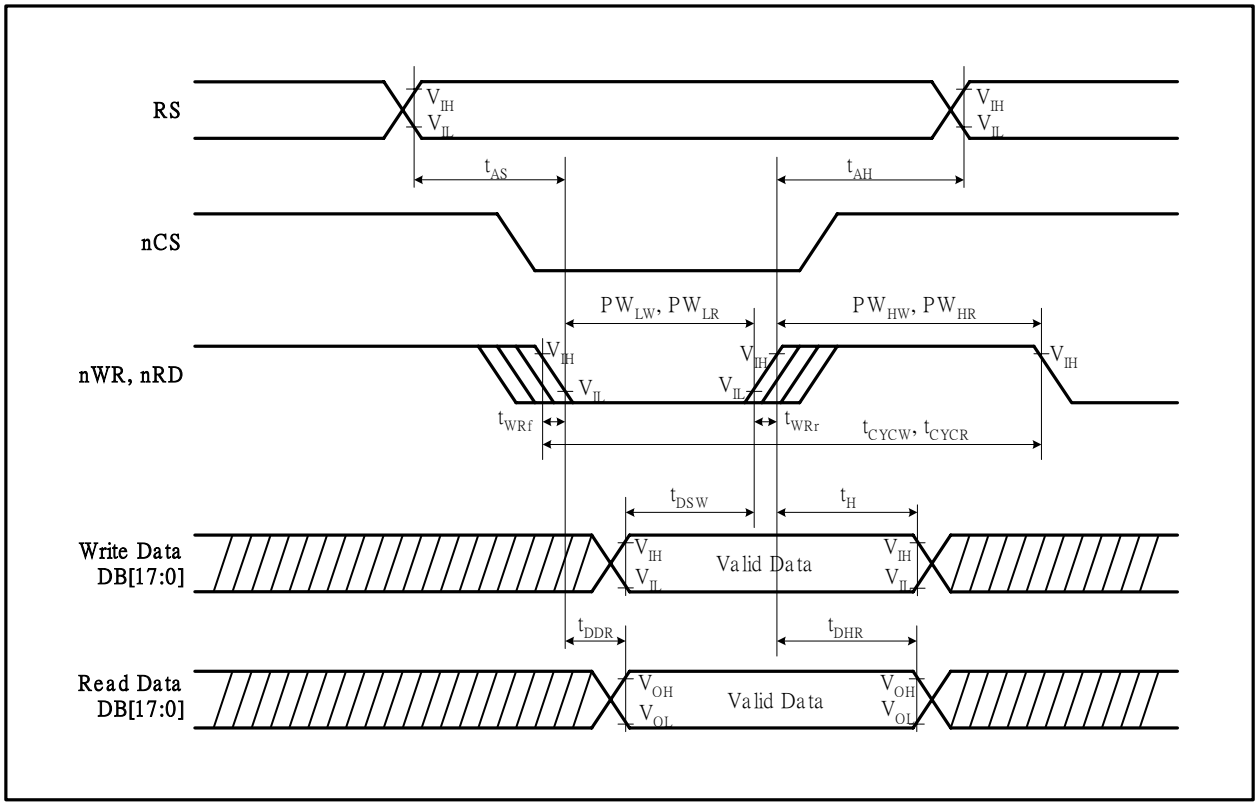


Figure 48 i80-System Bus Timing

14.4.2. Serial Data Transfer Interface Timing Characteristics

(IOVCC= 1.653.3V and VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	ns	100	-	-	
	Read (transmitted)	t_{SCYC}	ns	200	-	-	
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	-	
	Read (transmitted)	t_{SCH}	ns	100	-	-	
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	-	
	Read (transmitted)	t_{SCL}	ns	100	-	-	
Serial clock rise / fall time		t_{SCr}, t_{SCf}	ns	-	-	5	

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Chip select set up time	t_{CSU}	ns	10	-	-	
Chip select hold time	t_{CH}	ns	50	-	-	
Serial input data set up time	t_{SISU}	ns	20	-	-	
Serial input data hold time	t_{SIH}	ns	20	-	-	
Serial output data set up time	t_{SOD}	ns	-	-	100	
Serial output data hold time	t_{SOH}	ns	5	-	-	

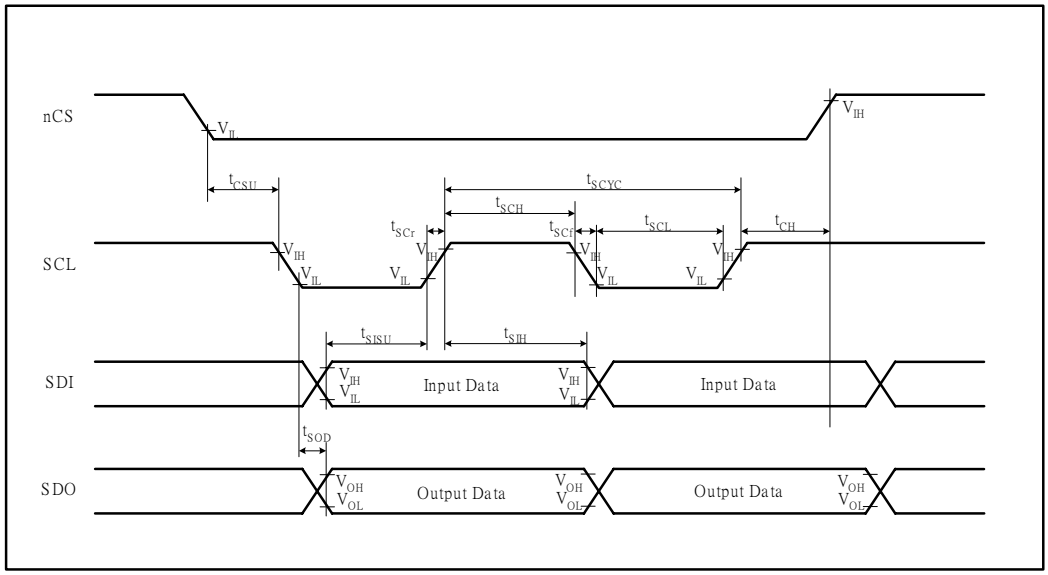


Figure 49 SPI System Bus Timing

14.4.3. RGB Interface Timing Characteristics

18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	30	-	-	-
DOTCLK high-level pulse width	PWDH	ns	30	-	-	-
DOTCLK low-level pulse width	PWDL	ns	30	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	80	-	-	-

DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

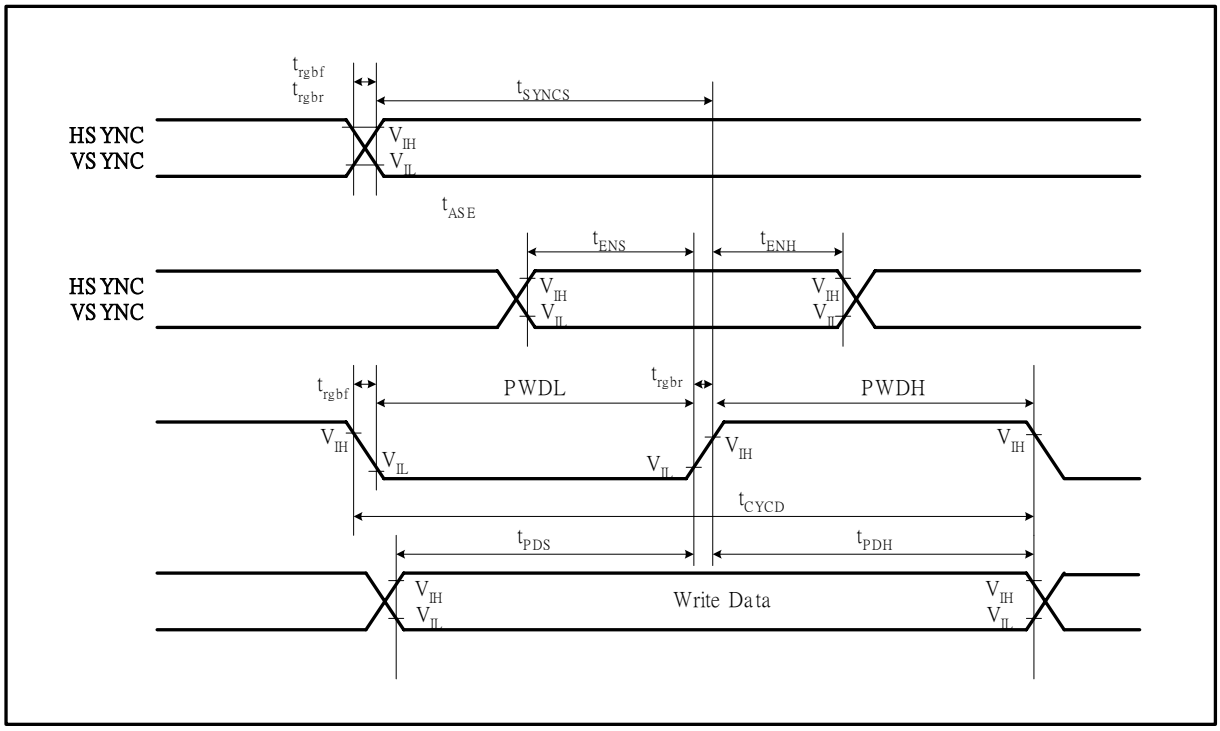


Figure50 RGB Interface Timing

14.4.4. MDDI Interface Timing Characteristics

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.
Data transfer rate	$1/t_{BIT}$	Mbps	Figure 51	10	70	130[Note2]
Differential transfer input skew	|±Tskew-pair-i|	ns	Figure 51	–	–	0.25
Data-stb input skew	|±Tdiff-pair-i|	ns	Figure 51	–	–	1.0

Note1: Set register R713h =0080h to adjust the bias current to reduce the power consumption, when the transfer speed request is slower than 130Mbps.

Note2: Set register R713h =0000h (default) to adjust the bias current, when the transfer speed request is between 130Mbps ~ 250Mbps.

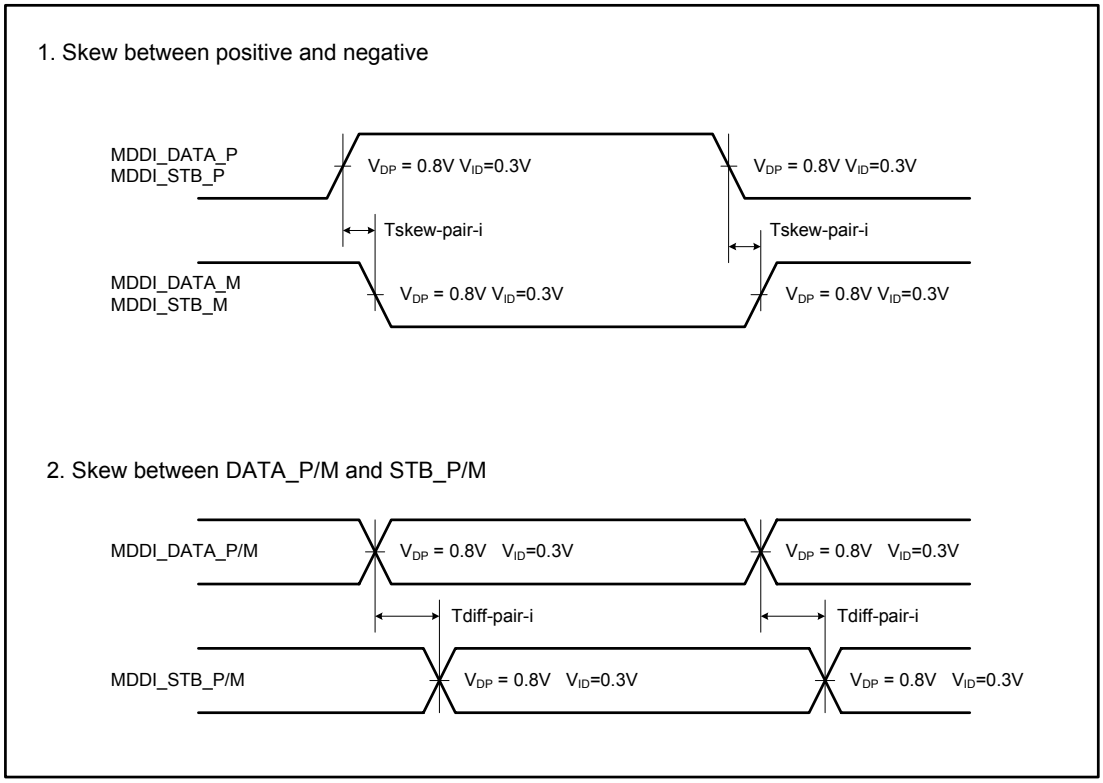


Figure51 RGB Interface Timing

15. Revision History

Version No.	Date	Page	Description
V.01	2006/4/17		New Created
V0.12	2007/3/28	20	Modify pad name typing error.
V0.15	2007/4/30		Modify the BT[3:0] definition
V0.17	2007/7/12	19	Modify the pad coordination of S224 ~ S233
V0.20	2007/8/9	35	Add the MDDI interface
V0.23	2007/10/09	-	Remove VCMR and VCOMR function. Modify the MTP programming flow.
V0.24	2007/10/29	117 ~ 120 15	Modify the power on/off sequence Modify Chip Thickness 400um to 280um(typ.)
V0.25	2007/12/25	68	Remove the deep standby function (DSTB)
V0.26	2008/03/23	53, 58, 61, 62	Modify the register R22h to R202h.
V0.27	2008/06/28	63 124	Interface timing gate line number type error Delete LCD output Characteristic
V0.28	2008/07/24	48, 124, 128	Add the AC/DC characteristics for MDDI interface
V0.29	2008/10/31	71	Update the OTP programming voltage
V0.30	2009/06/08	68,88	Remove R102h PSON
		89	Add power control describe
		23	Delete Bit Operation function
		127	SPI Write/Read timing unit